Kaunas University of Technology

Faculty of Electrical and Electronics engineering

Investigation of High Voltage Pulsers for Ultrasound

Master's Final Degree Project

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Summary

The use of ultrasound in non-invasive research and measurements is a common practice in material science. To generate ultrasound ultrasonic transducers are needed, which are commonly made of piezoceramics. Because of the properties of piezoceramics, ultrasonic transducers made from it have a complex input impedance. Not all ultrasonic transducers are made of piezoceramics and alternative materials, such as ferroelectretics are used. The use of ferroelectretics allows to reduce the capacitance of the ultrasonic transducer. In many non-invasive ultrasonic tests, it is of the highest importance to achieve the greatest possible resolution. To achieve high resolution shorter ultrasonic wavelengths must be used, which means higher ultrasonic signal frequency. In many materials ultrasonic wave penetration depth decreases as the frequency increases. To be able to measure greater depth with a high frequency ultrasound, a higher energy signal is needed, which usually means high ultrasonic transducer excitation voltage. Another reason why it is important to have high voltage excitation signal is the high input impedance of the transducer. It is the main problem for ferroelectretic ultrasonic transducers, where the input impedance is higher than in piezoceramic transducers. In order to produce the same amount of acoustic energy as with piezoceramic ultrasonic transducers, excitation voltage must be increased, or a resonant frequency of the transducer used. The aim of this work is to investigate the high voltage pulsers used for ultrasonic transducer excitation. One of the tasks is to determine which of the pulser topologies is best suited to achieve high voltage, high frequency output signal. The comparison of the topologies will be made using several key parameters. Out of the tested topologies one will be chosen to be the main contender for achieving high voltage, high frequency output signal. It is also one of the tasks to evaluate the usage of gallium nitride transistors over silicon transistors. Gallium nitride transistors excel at having higher electron mobility, breakdown voltage and lower main channel conductance. By implementing gallium nitride transistors, the maximum pulser output frequency can be increased to 37 MHz for lower capacitance load of 470 pF and to 15,7 MHz for 2 nF load.

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Santrauka

Ultragarso taikymas neinvaziniuose matavimuose bei tyrimuose yra itin paplitęs medžiagų moksle bei medicinoje. Tam naudojami įvairūs ultragarsiniai keitikliai, kurių dauguma pagaminti iš pjezokeraminės medžiagos. Dėl šios medžiagos, ultragarsiniai keitikliai pasižymi kompleksiniu impedansu. Tačiau ne visi ultragarsiniai keitikliai yra pagaminti iš pjezokeramikos, yra naudojamos alternatyvios medžiagos, tokios kaip feroelektretai. Ši medžiaga leidžia sumažinti keitiklių talpumą. Skirtinguose neinvaziniuose ultragarsiniuose matavimuose norima išgauti kaip įmanomą didesnę skiriamąją gebą. Norint tai pasiekti reikia mažinti ultragarso bangos ilgį, kas reiškia ultragarso dažnio aukštinimą. Daugelyje tiriamųjų medžiagų didėjant ultragarso dažniui, ultragarso skverbtis mažėja ir signalas nepasiekia norimo gylio. Norint pasiekti reikiamą skverbties gylį, reikia didinti signalo energiją, kas įprastai reiškia ultragarsinio keitiklio žadinimo įtampos kėlimą. Kita priežastis, dėl kurios norima pakelti žadinimo įtampą – aukštas ultragarsinio keitiklio impedansas. Tai ypatingai aktuali problema feroelektretiniuose ultragarsiniuose keitikliuose, kur impedansas gali būti žymiai didesnis nei pjezokeraminiuose keitikliuose. Todėl norint išgauti tokią pat akustinę energiją kaip ir su pjezokeraminiais keitikliais, reikalinga didinti žadinimo įtampą arba pasinaudoti keitiklio rezonansu. Šio darbo tikslas - ištirti aukštos įtampos impulsų generatorius, naudojamus ultragarsinių keitiklių žadinimui. Nustatyti kurios topologijos schemotechninis sprendimas yra tinkamiausias generuoti aukšto dažnio, aukštos įtampos impulsus. Taip pat įvertinta galimybė pagerinti impulsų generatoriaus pagrindinius parametrus pasinaudojant naujos kartos galio nitrido tranzistoriais, kurie pasižymi geresniais elektronų judrumo, pramušimo įtampos, kanalo laidumo parametrais nei įprasti silicio tranzistoriai, kurie plačiai naudojami tiriamose topologijose. Aukštos įtampos impulsų generatoriaus atkuriama dažnių juosta praplatėjo iki 37 MHz, esant žemoms talpinėms apkrovoms, bei iki 15,7 MHz esant 2 nF apkrovai.

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List of abbreviations

Abbreviations:

CMUT – Capacitive Micromachined Ultrasonic Transducer;

CPLD – Complex Programmable Logic Device;

DC – Direct Current;

DUT – Device Under Test;

JFET – Junction Field-Effect Transistor;

IC – Integrated Circuit;

eGaN – Enhancement-mode Gallium nitride;

FET – Field-Effect Transistor;

FFT – Fast Fourier Transform;

GaN – Gallium nitride;

MOSFET – Metal-Oxide-Semiconductor Field-Effect Transistor;

PCB – Printed Circuit Board;

RMS – Root Mean Square;

SiC – Silicon carbide;

SJ – Super Junction;

STD – Standard Deviation;

SWC – Sine Wave Correlation;

Introduction

Ultrasonic based measurement is a common method for non-invasive investigation in medical science, material science and quality assurance in the manufacturing sector. Important factor of the ultrasonic measurements is the resolution. Resolution is directly proportional to the ultrasonic frequency used in taking the measurements [1, 2]. But in many cases, the higher the frequency, the lower the penetration depth to the test material of the ultrasound is. To achieve better ultrasonic penetration into a material, high power signals are needed [3]. This usually means increasing the excitation signal voltage. Another importance of high voltage pulsers is the necessity in driving high impedance ultrasonic transducers [4, 5] to achieve high acoustic power necessary for the material under test [6, 7, 8]. In most cases, the excitation signal can be a pulse train or a chirp signal [9, 10], [11, 12]. The pulser must be able to generate high voltage (>100 V) and high frequency (>10 MHz) signals when loaded with a capacitive load, which is present in all ultrasonic transducers [13]. Very high frequencies of more than 100 MHz can be used for ultrasonic transducer excitation, although it comes at a price of a very low voltage output (<2 V) [14]. In rare cases, the ultrasonic transducer must be excited with a voltage of 2 kV or even higher [15]. For many research purposes a bipolar output pulse is preferred [16]. In modern use of ultrasonic measurement systems, the most important factors, apart the actual imaging capabilities, are the abilities to be battery powered, be energy efficient and have a small footprint.

Some improvements over current pulser designs can be made by implementing GaN or SiC transistors. The new generation of GaN and SiC transistors offer better electron mobility, lower input, and output capacitances [17]. For a long time, the nature of GaN FETs were a challenge, as the transistors were working in depletion mode [18]. In order to have an enhancement mode GaN transistors, they were cascoded with silicon MOSFETs [19, 20]. Gallium nitride transistor excel at having lower conductance and switching losses [21, 22]. When the switching frequency is significantly higher (>30 MHz), every parasitic parameter of the PCB and the component influence the performance of the pulser [23, 24], and actions to mitigate them are of the highest importance.

The aim of this work is to investigate the high voltage pulsers and suggest key parameters for topology comparison. Make observations on improving current design by implementing new generation transistors. The objectives of the work are as follow:

- Analyse the currently in use pulser topologies, highlight their strong and weak points.
- Analyse the use of GaN and SiC transistors in switching applications and the main parameters.
- Make experiments to compare different topologies with different key parameters of interest.
- For the selected topology make comparison with the use of GaN or SiC FETs.

1. High voltage pulse generators

For the excitation of the ultrasonic transducers high voltage pulses are used. Devices called pulsers are used in generating a signal of a set waveform, frequency, and voltage [9, 10]. The main criteria for these devices are their output signal frequency capabilities, energy used to create output signals, distortion of the signal when loaded with various ultrasonic transducers. Different transducers have their own specific resonance frequency and different impedance curves [25]. The main topologies with their pros and cons are presented in (Table 1.1).

Table 1.1 Overview of topologies [9]

	Half-bridge	**B, AB amplifier**	**D, DE amplifier**	**Transformer push-pull**
Maximum output frequency	High	Medium	High	Medium
Bandwidth of the output signal	Wide	Wide	Narrow	Medium
Output power	High	Medium	High	High
Efficiency	Medium	Medium	High	High
Complexity of the circuit	Medium	Medium	High	Medium
Physical size	Small	Medium	Big	Medium
High voltage supply needed for bipolar output signal	Bipolar	Bipolar	Bipolar	Unipolar

1.1. Ultrasonic transducers

Mostly all ultrasonic transducers used in medical diagnostics, industrial applications and research have a dominant capacitive element. Depending on the technology of the ultrasonic transducer this capacitive part can be as little as just few tens of picofarads up to several thousands of picofarads [11]. Regardless of this capacitance, the pulser output must charge it to produce a valid output signal. In general, the energy used by the capacitive load can be found with Formula (1.1).

$$E_{HV} = V_{HV}^2 \cdot C_0, \tag{1.1}$$

If: E_{HV} – energy stored in the capacitor; V_{HV} – voltage on the capacitor; C_0 – capacitance of the capacitor.

The transducer equivalent circuit can be expressed by *Butterworth-Van Dyke* model (Fig. 1.1). A typical piezoceramic ultrasonic transducer has main capacitive element *C0*. But parallel to this, an *RLC* element is also present. This lumped parameter model is responsible for setting the transducer model with the right resonance frequency and the impedance curve.

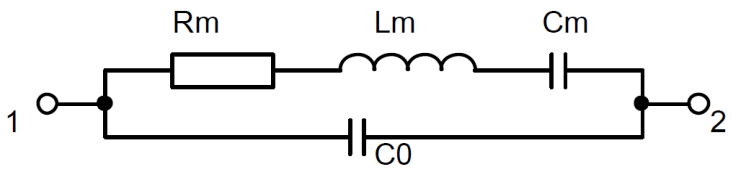

Fig. 1.1. Equivalent ultrasonic transducer model by *Butterworth-Van Dyke* [26]

1.2. Half-bridge topology based pulser

Half-bridge topology excels at excellent frequency response characteristics [10, 13] and low output signal distortions. The main drawback of this topology is its more complex MOSFET gate driving due to floating source voltage of the high side switch [12]. In order to successfully drive the high-side N-type switch, a dedicated high side driver must be used (Fig. 1.2), which usually implement an isolated DC/DC converter. Because of the nature of a DC/DC conversion circuitry, switching noise can affect subsequent signal acquisition systems with its electromagnetic interference. As an alternative, a boot-strap power supply can be used for the gate driver. By having additional circuitry in driving the high side switch, an extra delay time is added for this side. Thus, non-symmetrical output signal is generated. For this reason, the switching of the high and low side switches is required accordingly, or alternatively using the same circuitry for the low side switch to induce the same amount of delay to the low side. This longer delay compared to the other topologies is one of the main drawbacks of this topology. Another downside of using the dedicated floating voltage high-side gate drivers is the ability to only achieve up to mid-range frequency (around 10 MHz) [27], which is due to limitations by the driving circuitry itself [28]. This becomes more of an obvious problem when high voltage output is needed, as many devices are not designed for more than 100 V [27].

Another limiting factor for any topology is the maximum rated voltage of the transistor. For general silicon MOSFETs they can only achieve only up to 1200 V without compromising the switching characteristics of the transistor [28]. In some cases, for ferroelectretic ultrasonic transducers an excitation voltage of 2 kV is needed [5] thus requiring an adequately rated switch. When using a bipolar voltage source, the switches must be rated at least two times the voltage used for the output stage [34].

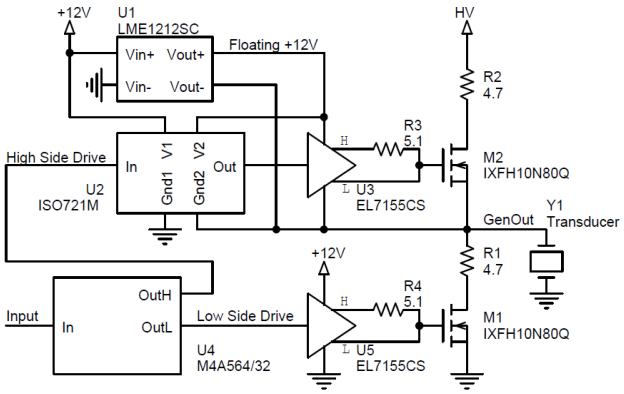

Fig. 1.2. Half-bridge topology with isolated high side gate driver [10]

The efficiency can then be easily expressed as a ratio between the power used by charging the capacitor of the ultrasonic transducer, and the total power used up by the high voltage source [11]. In theory, as the efficiency of the system gets better, the output capacitance the main switches decrease. The efficiency of the output stage will be researched in this paper by experimenting with more efficient, new generation transistors with much lower input and output capacitances and other key parameters.

1.3. Transformer gate-drive topology based pulser

Before isolated gate driving circuits became available, transformer gate drive topology was widely used to drive transistors [27] in half-bridge configuration (Fig. 1.3). As discussed in the previous section, isolated drivers have several drawbacks, but by using transformer isolation for the gate of the MOSFET, very little propagation delay can be observed. In advance, by using a transformer, a more variable gate driving voltage can be achieved and a more optimal driving point can be found.

The main object of concern for this topology is the transformer itself. In real case no transformer is ideal, and losses occur. One part of the losses is the energy stored in transformer's core. This can be taken in consideration with introducing leakage inductance. Another point to consider is that the transformer core tends to saturate when low frequency signal is passed through [9, 13]. Transformer gate-drive topology is not suitable for low frequency signals.

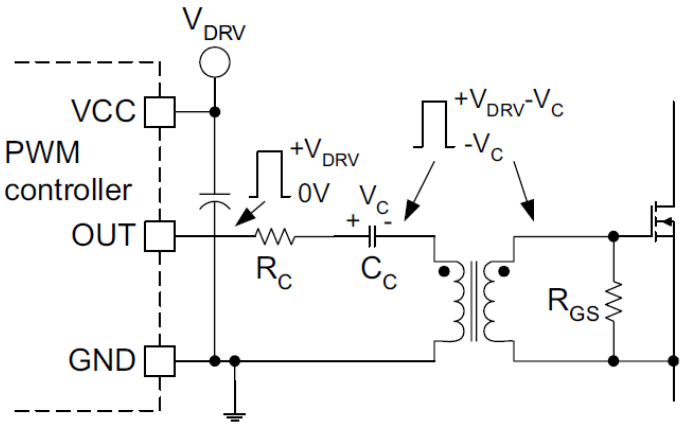

Fig. 1.3. Transformer gate drive topology [29]

The transformer coupling ratio can be determined by using formula (1.3). For calculating the mutual inductance, Formula (1.2), transformer coils must be connected in series for the first measurement and then one of the coils flipped and measured again.

$$M = \frac{1}{4}\left(L_{series+} - L_{series-}\right), \tag{1.2}$$

If: M – mutual inductance; $L_{series+}$ – inductance of transformer coils in series; $L_{series-}$ – inductance of transformer coils in series with reversed order of coils in series.

$$k = \frac{M}{\sqrt{L_p L_s}}, \tag{1.3}$$

If: k – transformer coupling ratio; M – mutual inductance; L_P – inductance of the primary coil; L_S – inductance of the secondary coil.

It is necessary to consider the capacitor C_C to avoid any residual DC current flow through the primary winding of the transformer. This can lead to the saturation of the transformer core [13], thus making the circuit unable to control the switches and distorting the output signal [29].

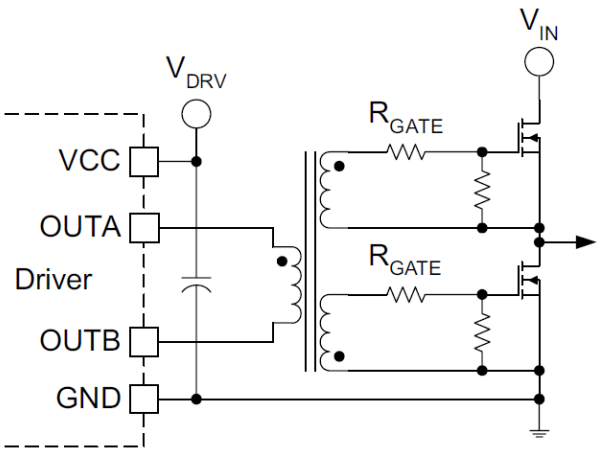

Fig. 1.4. Simultaneous high and low switch driving using a transformer [13]

By using a transformer to drive the transistor gate, an advantage of adding multiple secondary coils can be used to drive both switches with only one driver (Fig. 1.4). It is worth noting that by implementing this technique the leakage inductance increases, thus reducing the maximum achievable frequency. Also, this requires a gate driver with enough sink and source current capabilities as the primary winding must carry enough current for both switches. The main disadvantage of this technique is not being able to insert dead time between closing of one switch and opening of the other. This can lead to increased power consumption (Fig. 1.5) because of the simultaneous semi-open states of both switches during the changing of their states [10, 30].

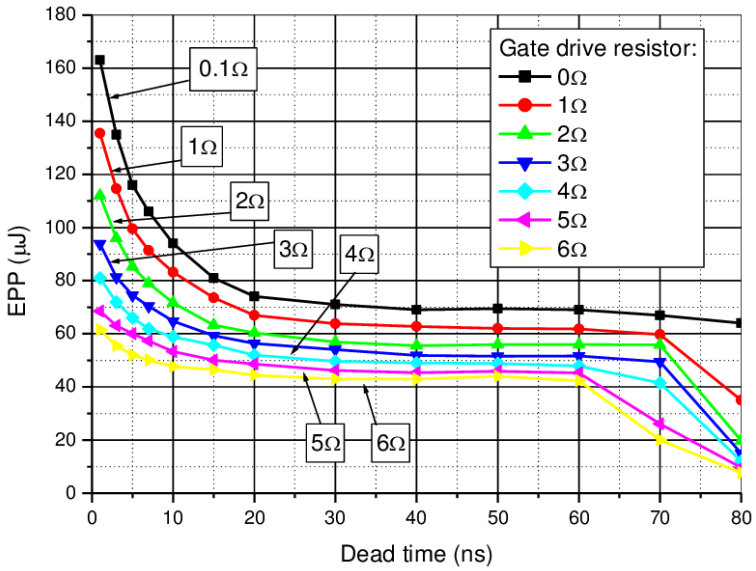

Fig. 1.5. Energy used per pulse vs dead time for 5 MHz signal, no load [10]

From the research done in paper [10], it is notable that by removing dead time from switching of the MOSFETs, an increase of 100 % can be seen in used energy per pulse. Increasing the resistance of the external gate resistor also lowers the used energy to produce a pulse by mitigating ringing, occurring on the gate of the MOSFET.

1.4. Push-pull topology pulser

Push-pull topology allows to achieve frequencies beyond 20 MHz [1, 3]. It also has one advantage over other topologies that is to form a bipolar signal at the output, only a single unipolar voltage supply is needed. As is in any case when using a transformer, transformer core saturation must be considered. Saturation can occur when a low frequency pulses or a longer high frequency pulse trains are passed through the transformer [11]. Saturated core eliminates the inductance of the coils thus making the transformer inactive. To reduce this problem, a second secondary coil is added to the transformer (Fig. 1.6). By using the switches M_3 and M_4, this coil can be made into a closed loop, thus discharging the energy, stored in the core of the transformer [31].

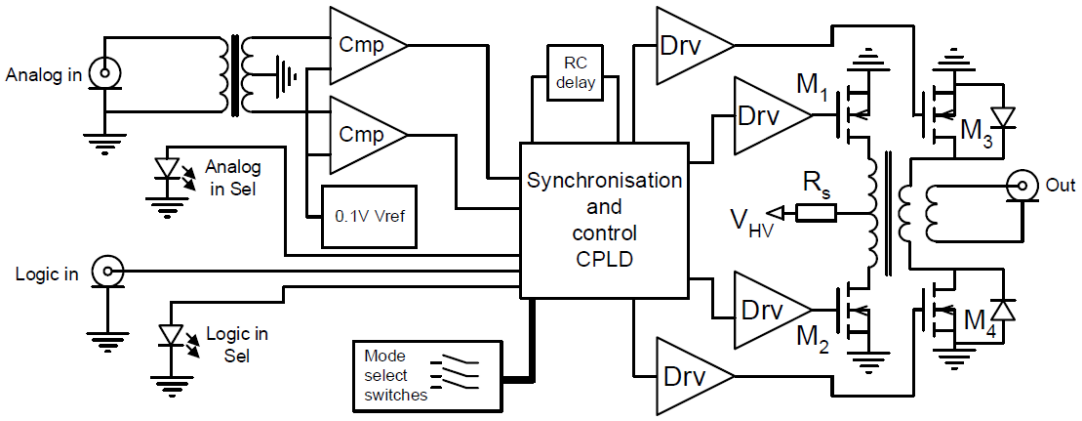

Fig. 1.6. Transformer push-pull topology pulser [31]

From research done in papers [13, 31], push-pull topology was tested with different frequency pulse trains (Fig. 1.7). The transformer used in this experiment showed signs of saturation at 2 MHz signal, when the first half-period of the pulse is distorted. When signal frequency increases, a more obvious signal distortion is observed. The output signal is no longer a square signal but a triangle. This is explained because of the nature of the output stage, it forms an *RLC* circuit. The circuit acts as a low-pass filter, reducing the amplitude of the harmonics of the square wave signal. For the capacitive element, the main contributor is the output capacitance of the MOSFETs used [32]. This circuit does not only provide a pulser with an unnecessary low-pass filter on the output stage, but also provides a resonance of the output at a specific frequency which is determined by the *RLC* circuit component values.

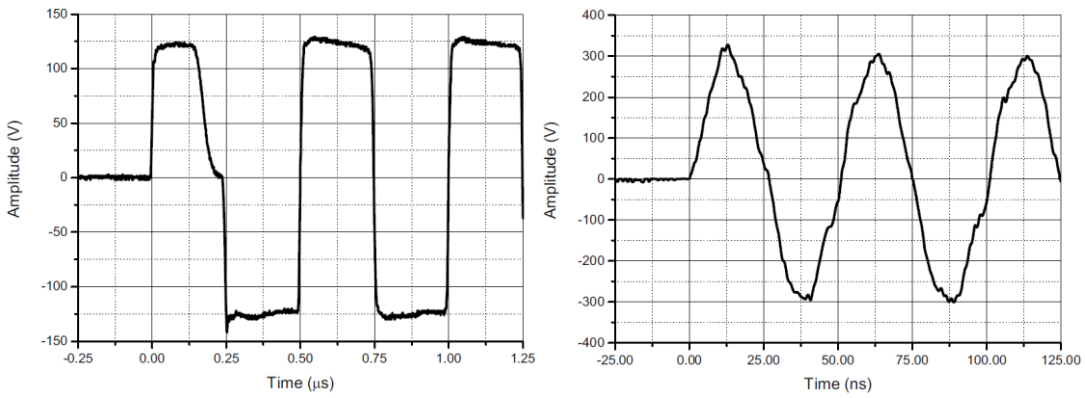

Fig. 1.7. Output signals of 2 MHz (left) and 20 MHz (right) pulses of a push-pull topology [13]

When using a push-pull topology it is recommended [1] to use a snubber circuit (Fig. 1.8). Snubber circuit is an *RC* filter used to filter out oscillations that occur when turning the switch on or off. The cause of the oscillations (Fig. 1.9) is due to the parasitic components of the transformer windings, mainly the leakage inductance, and other part is due to the parasitic inductances of the printed circuit board tracks, pins of the MOSFET, transformer. The capacitive part of the oscillator is the output capacitance of the MOSFET used [32] and any additional parasitic capacitance of the output PCB tracks. The optimal snubber circuit parameters can be calculated by Formula (1.4) [32]. The capacitance of the snubber circuit is chosen depending on the desired speed of the switching of the MOSFET and the allowed energy losses, that are unavoidable in this circuit.

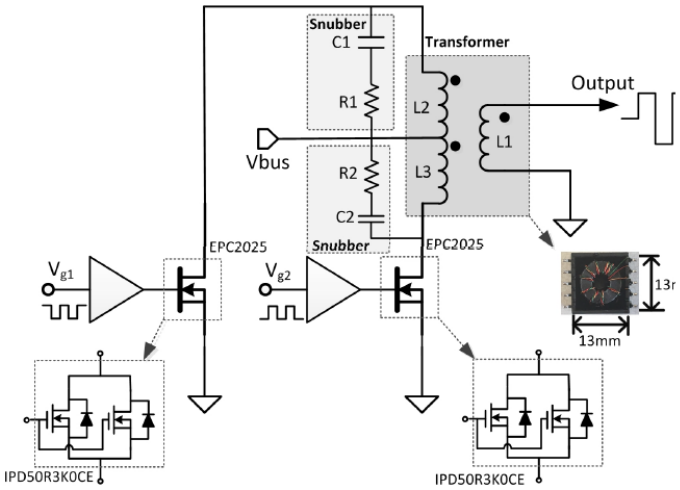

Fig. 1.8. Push-pull topology with snubber circuit and employing a GaN transistor EPC2025 [1]

$$R_1 = \sqrt{\frac{L_{leak}+L_{par}}{C_{OSS}}}, \tag{1.4}$$

If: R_1 – resistance of the snubber resistor; L_{leak} – leakage inductance; L_{par} – parasitic inductance.

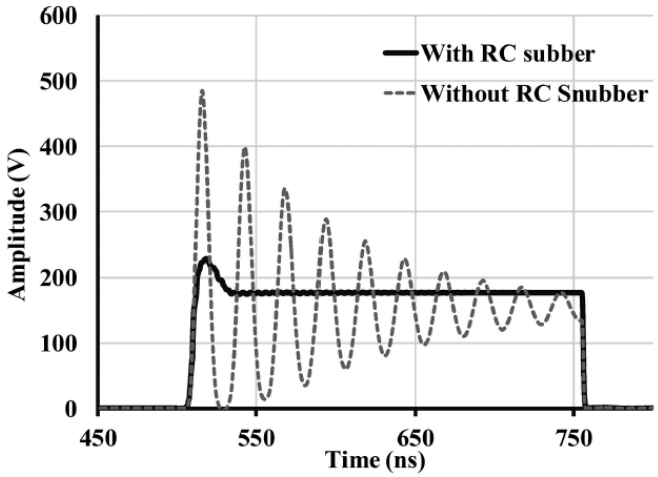

Fig. 1.9. Effect of a snubber circuit on the gate of the transistor [1]

1.5. Resonant gate drive topology

One of the main contributors to wasting energy when switching the MOSFETs is the gate charging. Every MOSFET has an input charge and an equivalent capacitance, which needs to be charged in order for it to open and conduct electric current through the drain-source channel. This charging of the gate charge is wasteful, especially for MOSFETs switched at higher frequencies, as the wasted energy is directly proportional to the switching frequency [35]. The use of resonant gate driving allows to take back part of the energy used to charge the gate and reuse it in the next cycle [36].

To reduce this wasted energy a resonance gate driving can be implemented. This requires lower power switches for the gate driving, an inductor and synchronization from a controller. The resonant gate driving for a single period is made of four steps (Fig. 1.10).

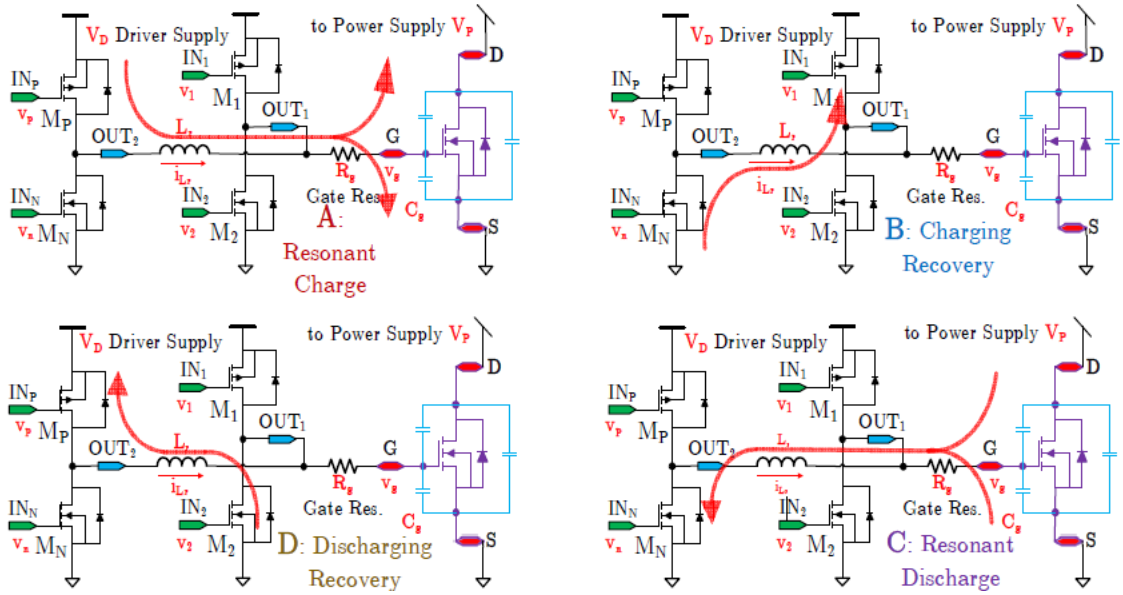

Fig. 1.10. Stages of resonant gate driving [35]

In the paper [35], the proposed resonant gate driving circuit is used (Fig. 1.10). In the first stage, the switch M_P is turned on and the current charging the input capacitance of the main MOSFET flows through the inductor L_r (Fig. 1.10 A). After the initial charging of the input capacitance of the MOSFET, the switch M_P is turned off and switch M_1 is turned on (Fig. 1.10 B). This allows the energy stored in the coil to be transferred to drive supply capacitors through the low impedance path of M_1. To turn off the main MOSFET switch M_N is turned on and the charge from the input capacitance of the MOSFET flows through the coil (Fig. 1.10 C). After discharging the input capacitor switch M_N is turned off and switch M_2 is turned on to store the energy of the coil to the supply source (Fig. 1.10 D).

As the name implies, it is a resonance-based gate driving, meaning it can only operate at a specific set resonance frequency with a very narrow bandwidth. This method would not be suitable for frequency sweep signals, such as chirp. The resonance frequency is set by the transistor input capacitance and the coil used to form the *LC* tank circuit. Also, this method is not efficient for producing short pulse train signals of low repetition frequency, making the gate driving circuitry complex without significant energy efficiency, which can be achieved for continuous wave signal.

2. New generation of high-speed transistors

For every high voltage pulser topology, discussed in the previous chapter, the most important part is the high voltage switch. Depending on the task that is required from the pulser, choosing the right switch is very important. One task might require low frequency but high current capabilities, and another task might require very little current but high frequency capabilities or be able to handle very high voltages. For all these different tasks, an adequate power switch must be chosen to suit requirements for each task as the switches themselves can have very different parameters depending on their developed use. The improvements in power switch technology have increased tremendously over the last decade. Now, new transistors made from gallium nitride or silicon carbide are widely available and offer better switching capabilities compared to their silicon counterparts [42]. Even the switching capabilities of silicon transistors have been enhanced by reducing the parasitic components of the transistors by improving the manufacturing technologies [37, 38, 39].

The main parameters of a semiconductor transistor are, for example, maximum operating voltage, input, output capacitance, reverse recovery capacitance and gate charge. Many of these parameters are directly related to the switching speed capabilities of the switch. When using an equivalent MOSFET model (Fig. 2.1), the parasitic capacitances can be expressed as shown with Formulas (2.1 – 2.3) [29].

$$C_{iss} = C_{gd} + C_{gs}, \tag{2.1}$$

$$C_{oss} = C_{gd} + C_{ds}, \tag{2.2}$$

$$C_{rss} = C_{gd}, \tag{2.3}$$

If: C_{iss} – input capacitance; C_{gd} – capacitance of gate-drain; C_{gs} – capacitance of gate-source; C_{oss} – output capacitance; C_{ds} – capacitance of drain-source; C_{rss} – reverse transfer capacitance.

For regular silicon MOSFETs, the main area of concern for achieving the highest possible switching speed is gate charge and input capacitance. These parameters must be taken into consideration when choosing a gate driver, which directly determine the maximum gate charge current and minimum rise time.

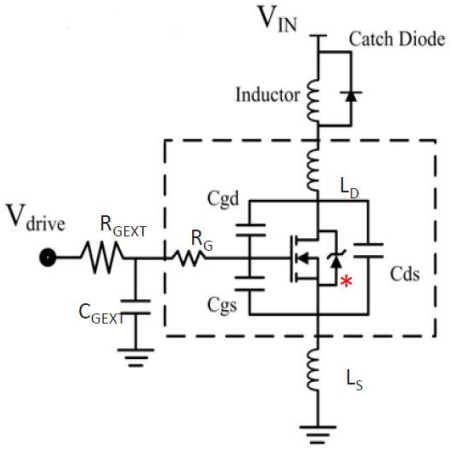

Fig. 2.1. Equivalent model of a silicon MOSFET [29]

The input and output capacitances of a MOSFET depend on the voltage applied to the drain-source of the MOSFET (Fig. 2.2). Generally, the higher the applied voltage, the lower these parasitic capacitances become, which is due to the narrowing of the semiconductor junction when the electric field strength increases. The general equations for the input capacitance components of the silicon MOSFET are Formulas (2.4) and (2.5) [29].

$$C_{gs} = \frac{C_{gs}(0)}{\sqrt{1-\frac{u_{gs}}{U_d}}}, \tag{2.4}$$

$$C_{gd} = \frac{C_{gd}(0)}{\sqrt{1-\frac{u_{gs}}{U_d}}}, \tag{2.5}$$

If: C_{gs} – capacitance of gate-source; u_{gs} – gate-source voltage; U_d – drain voltage; C_{gd} – capacitance of gate-drain.

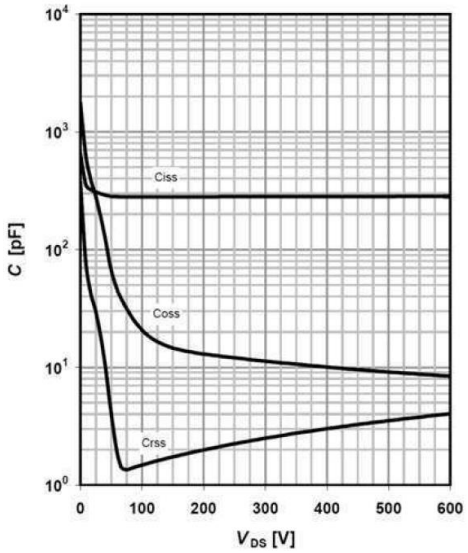

Fig. 2.2. Typical curves of the capacitance vs applied voltage (IPD60R2K0C6)[1]

In the industry, a parameter of figure of merit is used to express the electrical conductance losses and dynamic losses of a switch by using Formula (2.6) [40]. Equivalently, a figure of merit can express the losses regarding the gate charge value, Formula (2.7).

$$FOM = C_{OSS\_eqv} \cdot R_{DS}\ , \tag{2.6}$$

$$FOM = Q_G \cdot R_{DS}\ , \tag{2.7}$$

If: *FOM* – figure of merit; C_{OOS_eqv} – equivalent output capacitance; R_{DS} – resistance of drain-source; Q_G – gate charge.

To reduce the dynamic losses of a switch, newer semiconductor technologies have been developed. Gallium nitride and silicon carbide semiconductor switches offer lower parasitic capacitances and charges, thus making faster switching speeds possible [40]. These new semiconductor materials allow for better electron mobility, higher breakdown voltages and lower turn on threshold compared to regular silicon technology (Table 2.1).

[1] https://www.infineon.com/cms/en/product/power/mosfet/500v-900v-coolmos-n-channel-power-mosfet/600v-coolmos-n-channel-power-mosfet/ipd60r2k0c6/

Table 2.1. Properties of the semiconductors used in power switches [40]

Parameter	GaN	Si	SiC
E_G, eV	3,4	1,12	3,2
E_{BR}, MV/cm	3,3	0,3	3,5
V_S, x10^7cm/s	2,5	1,0	2,0
μ, cm^2/V_S	990-2000	1500	650

One of the main advantages of silicon carbide and gallium nitride semiconductor material is the much higher breakdown voltage, which allows reducing the die size and still maintaining the rated voltage limit. Due to smaller die size, the parasitic capacitance and inductance are decreased. The higher electron mobility allows for lower drain-source resistance as well as lower internal gate resistance [38, 39, 40]. When considering high voltage transistors, compared to similarly rated pure silicon MOSFETs, silicon carbide can offer switches with a maximum rated voltage of up to 3.5 kV, without sacrificing the high-speed switching capabilities [37, 41]. More detailed parameters of GaN, SiC and Si semiconductors are shown in (Table 2.2).

Table 2.2. Comparison of transistors with different semiconductor technologies [37]

	SiC Cascode UJC06505K	SiC MOSFET SCT3120KL	E-mode GaN GS66508B	Si Superjunction IPP65R045C7
R_{DSA}, mΩ/cm2	0.75	3.5	6.6	10
$R_{DS\cdot EOSS}$, mΩ/μJ	255	600	350	462
V_{TH}, V	5	4.5	1.3	3.5
Avalanche	Yes	Yes	No	Yes
Gate voltage rating, V	±25	+22/-4	±10	±20
Diode behaviour	Excellent	Excellent	Excellent	Poor

The obvious benefit of gallium nitride and silicon carbide semiconductor switches is the non-existing reverse diode, which is present in every silicon MOSFET. This diode and its additional reverse capacitance reduce the switching speed of the switch. Gallium nitride switches do not suffer from avalanche breakdown when overvoltage on drain-source occurs, giving them more immunity compared to other technologies [37, 39]. Gallium nitride switches also have the lowest turn-on threshold level, but also suffer from the lowest immunity to gate-source overvoltage [38, 43].

In the case of enhancement mode gallium nitride FET, a comparison with a silicon MOSFET has been made (Fig. 2.3) by comparing different loss components. From this chart an obvious lover loss in almost every field can be seen. In total, a decrease in energy losses of around 40 % can be observed. The lower losses allow for greater current to passed through, especially in pulsed mode, although excess current can lead to instability of the transistor [44]. When observing GaN transistor driving in high frequency pulse operation [45, 46], some challenges in driving half-bridge topology can occur, such as gate-source ringing [47] and the effect of fast transients on the transistor [48, 49, 50]. In many cases, just by increasing external gate resistance or using the snubber circuits, the oscillations can be dampened [51].

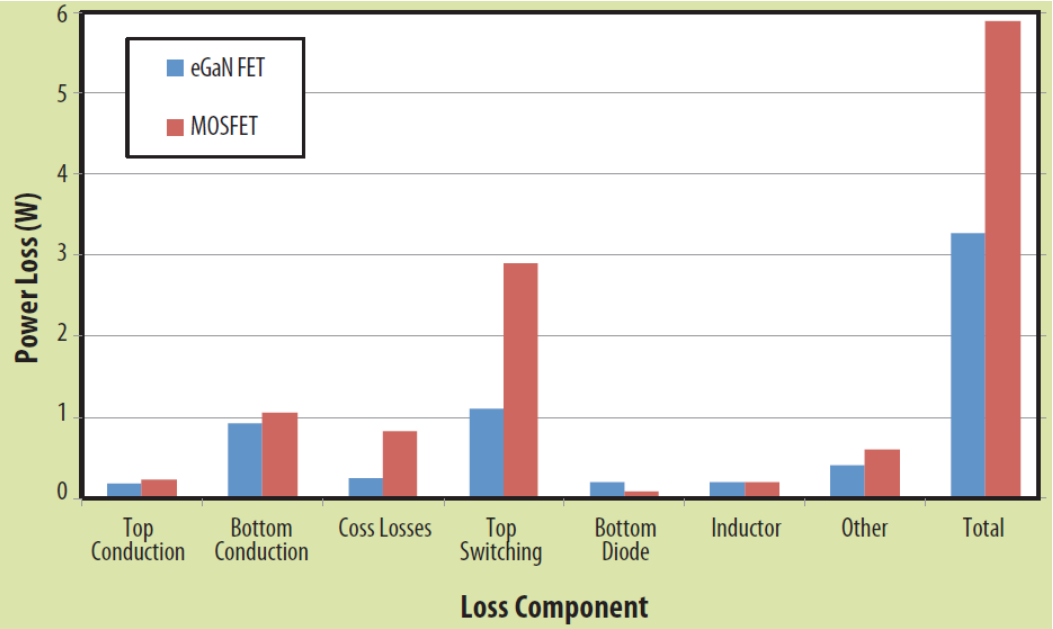

Fig. 2.3. Components of losses for enhancement mode eGaN FET vs Si MOSFET (at 1 MHz) [39]

In many cases, *GaN* transistors have a lower turn-on threshold voltage than regular silicon MOSFETs, and their absolute maximum rating for gate driving voltage is also lower, thus requiring extra attention when supplying gate control voltage. Another aspect of lower turn-on threshold is the lower propagation delay because the switch can be turned on by several hundreds of picoseconds or even several nanoseconds earlier.

Another advantage of transformer gate-drive topology comes to play: a custom transformer transmission ratio can be made to drive GaN FETs without compromising speed of the gate driving circuitry when using a lower voltage (Fig. 2.4). Many common gate-driving circuits have been optimized for 10 ÷ 12 V gate driving, although with the more common appearance of GaN transistors, specialized GaN transistor gate drivers are being developed and made available.

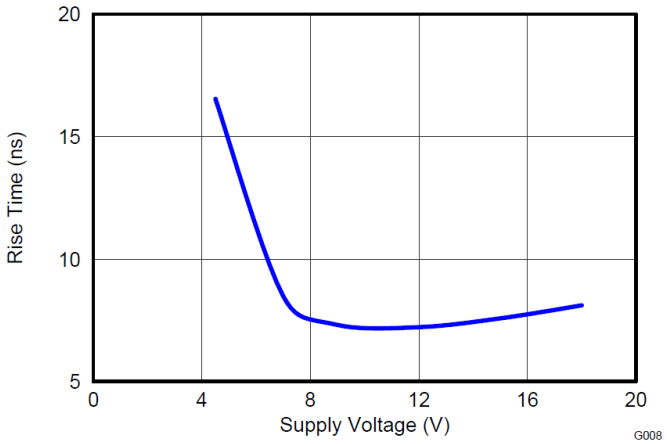

Fig. 2.4. Rise time vs supply voltage from ucc27511 datasheet[2]

[2] https://www.ti.com/product/UCC27511

3. Methodology for evaluating and comparing topologies and transistors

The aim of this work is to evaluate different pulser topologies. Also, one of the main tasks is to evaluate the use of gallium nitride transistors as a more efficient and faster alternative to the transistors currently in use in the pulsers under test. For this reason, key parameters must be chosen to be able to compare different topologies and determine their strong and weak points.

When taking measurements with ultrasonic systems, especially for battery operated devices, the energy used to produce the output signal is important and needs to be acknowledged. As is in many cases, the main point of a device is to have as high as possible efficiency to conserve energy and prolong the life of the device if it is operated by battery power. Power used only by the capacitive load with pulse train output signal can be calculated [10] using Formula (3.1).

$$P = E_{HV} \cdot PRF \cdot N\ , \tag{3.1}$$

If: P – power used by the capacitive load; E_{HV} – energy used per pulse; PRF – pulse repetition frequency (in Hz); N – number of pulses in a pulse train.

The main parameters for every piece of generator are its maximum values, in this case frequency, output voltage, propagation delay. Maximum achievable frequency can be estimated from the rise time [40] using formula (3.2).

$$f_{max} = \frac{1}{\pi \cdot t_{rise}}\ , \tag{3.2}$$

If: f_{max} – maximum estimated frequency; t_{rise} – rise time of a signal.

Maximum frequency can be determined by increasing the input signal frequency and observing the output signal of the pulser. To determine at what point the output signal is no longer viable for the purpose of the pulser, a simple maximum amplitude comparison can be used. The most common threshold for this is the -3 dB level. To measure the output signal amplitude and frequency several methods can be used. The most common method is to use Fast Fourier Transform (FFT) to get information about the frequency components of the signal, and their amplitude. The other method to use is the Sine Wave Correlation (SWC). The SWC method offers more precise assessment of signal amplitude and phase at a specific frequency. With this, a more accurate frequency value can be represented, compared to what can be achieved by using FFT with its limited frequency separability, regarding the frequency resolution of its nature. When determining the -3 dB point of the pulser output, the reference voltage (0 dB level) is set to the high voltage DC bus value. Using the SWC allows evaluating the maximum output frequency for a harmonic signal. In the case of this study, one of the objectives is to generate a square wave output. In trying to directly assess the maximum square wave output frequency, a correlation with an ideal square output signal can be used. The result of correlation between the pulser output and the ideal signal gives parametric value of how much the output signal of the pulser represents a square wave. In common cases, a correlation result value that is higher than 0.8 is considered a good match, while a result as low as 0.7 can be acceptable.

In telecommunications, peak-to-average power ratio or crest factor is often used [52], and it can be interpreted to describe signal's 'squareness'. It is expressed as a ratio between signal's peak and RMS value – Formula (3.3) [52]. The more the result is closer to 0 dB level, the more it is closer to the ideal shape of a bipolar square wave or a DC voltage.

$$PAPR = 10 \cdot log_{10} \frac{|x_{peak}|^2}{{x_{RMS}}^2}, \quad (3.3)$$

If: $PAPR$ – peak and RMS ratio of a signal; x_{peak} – signal peak value; x_{RMS} – signal RMS value.

Maximum working voltage is mainly limited by the power switches used in the pulse generator. All of them have a nominal breakdown voltage limit. The other factor limiting the maximum working voltage is the voltage transient effect on power switches when switching at high frequencies. With super-junction and gallium nitride transistors, the transient voltage immunity level can reach the value of 100 V/ns. For silicon carbide transistors, the transient voltage immunity level is much higher.

Propagation delay is measured as the time difference between the input excitation signal and the output signal (Fig. 3.1). The point of measurement is the 50 % mark of the rising edge for IN+ and OUT signals of the DUT.

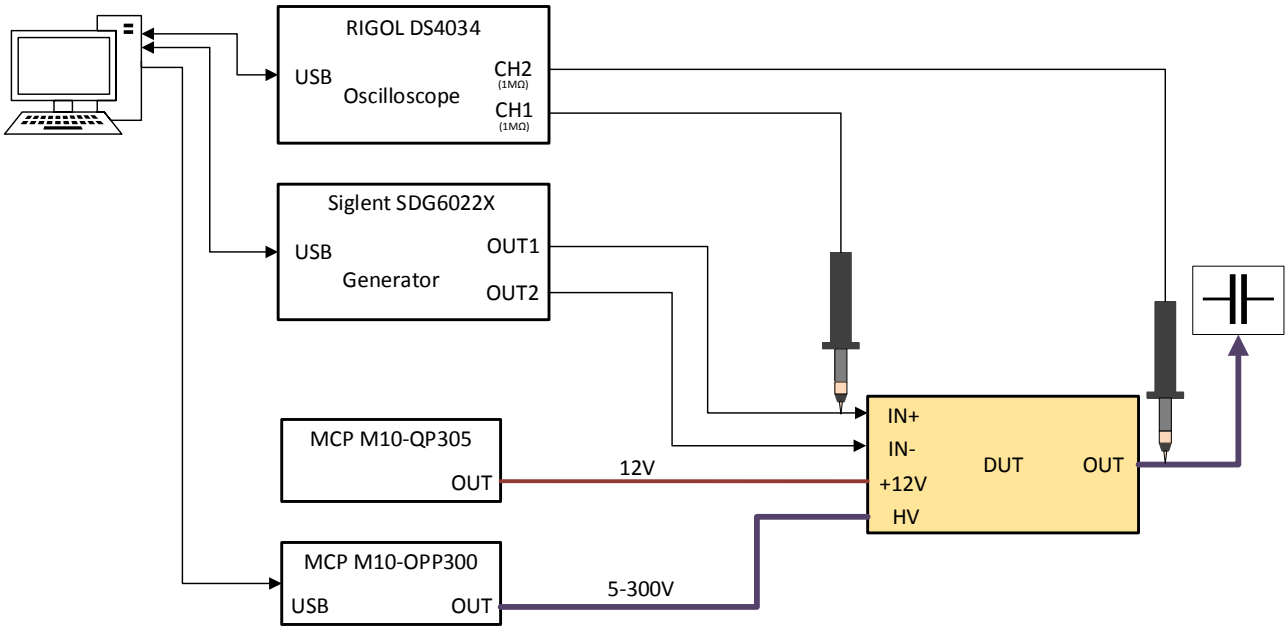

Fig. 3.1. Setup for measuring propagation delay

Signal waveform asymmetry can be determined by measuring pulse width, regardless of whether it is a positive or a negative half-period. In an ideal signal, a pulse width should be equal to half of the period of the signal. In this case the actual pulse width, measured from the captured oscilloscope data, is compared with a set pulse width value. While the output signal is still viable, a small deviation can be observed. But when greater drift from an ideal value is observed, the output signal no longer represents the wanted waveform, and it indicates a distortion. For this application, a deviation of up to 10 % can be considered acceptable.

As comparing pulse width of the output signal can indicate some degrees of distortions, another parameter to indicate a distortion can be the DC offset of the output signal. In an ideal case for a bipolar signal, this DC offset is 0 V, as the positive and the negative half-periods of the signal are equal in time width and amplitude. The DC component is measured from a windowed signal of an integer number of periods, in the case of this work – 5 periods. An increase or decrease of a DC component indicates the inability of the circuit to maintain the output signal.

4. Comparison of the high voltage pulsers

The main purpose of this work is to determine which of the presented high voltage pulser topologies can achieve the highest output frequency, as well as to determine strong and weak points of every pulser topology and its use case, based on previously set up criteria.

4.1. Simulation of the pulser topologies and switches

When simulating a circuit with a specialised simulation tool, it is important to represent the situation as closely as possible, to achieve results similar to real tests. One of the key parts in every topology under test is the gate driving integrated circuit. These ICs are not ideal and have different parameters to describe that, such as maximum operating voltage, maximum sink, source currents, rise and fall times, and transient voltage immunity. All of that must be taken into account when simulating the pulser, in a case that the gate driving IC has no available SPICE model. Parameters of gate-driving integrated circuits used in pulser under test and potential new candidates for use with GaN transistors are given in (Table 4.1).

Table 4.1. Parameters of gate-driving integrated circuits

Part name	Power switch	V_{max}, V	V_{cc_min}, V	V_{cc_max}, V	I_{sink}, A	I_{source}, A	T_{rise}, ns	T_{fall}, ns	T_{delay}, ns	I_q, μA	dv/dt, V/ns
LMG1020	MOSFET GaN FET	300	5.00	5.75	5	7	0.4	0.4	2.5	75	300
UCC27524	MOSFET IGBT	620	4.50	18.00	5	5	7.0	6.0	13	100	50
UCC27511	MOSFET IGBT	620	4.50	18.00	8	4	9.0	7.0	13	100	50
UCC21222	MOSFET IGBT GaN FET	990	9.20	18.00	6	4	5.0	6.0	28	1500	100

For transformers, a coupling ratio of 0.95 is taken as a base line, considering the results of the transformers measured in the lab. The coupling ratios for the transformers were calculated using (1.2) and (1.3) formulas for transformer gate drive and push-pull topologies. The average results for both transformers were close to 0.95.

Regarding the rise times of the gate drivers, a rise time for a typical gate as a load is in range from 5 ns to 9 ns. Faster rise times can be achieved with dedicated GaN FET drivers, although they do not meet the maximum voltage requirement. For the purpose of simulating a non-ideal signal, the rise and fall times of 5 ns and 6 ns will be set accordingly.

The half-bridge topology (Fig. 4.1) consists of only six main components: two MOSFETs, two external gate resistors and two resistors to limit the current on the output stage. The switches used in this simulation are IPD60R2K0C6 Si super-junction MOSFET and eGaN FET GS-065-004. Current limiting resistors are set to a value present in DUTs, which are 4.7 Ω. The high voltage supply is set to a maximum value of 300 V. The loads used in the simulations are: 50 Ω, 470 pF, 1 nF, 2 nF and 10 pF to imitate open output of the pulser with only some little value of parasitic capacitance present.

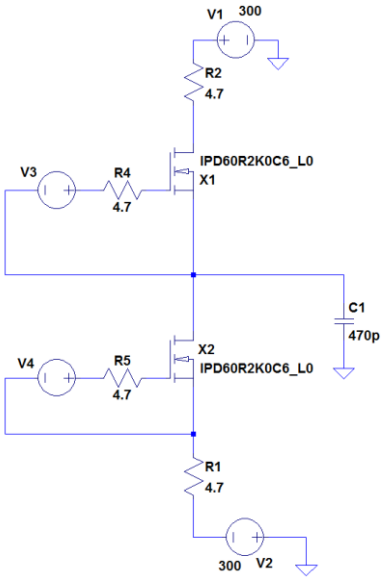

Fig. 4.1. Model used for half-bridge topology simulation

Transformer gate drive topology (Fig. 4.2) requires additional transformers when compared with half-bridge topology. The values for the coils of the transformer are found by measuring the transformer of the DUT, which will be tested in the next chapter. The coils of the transformer are measured, and the values are rounded to be 12 μH. The rest of the components are kept the same values as in previous simulation.

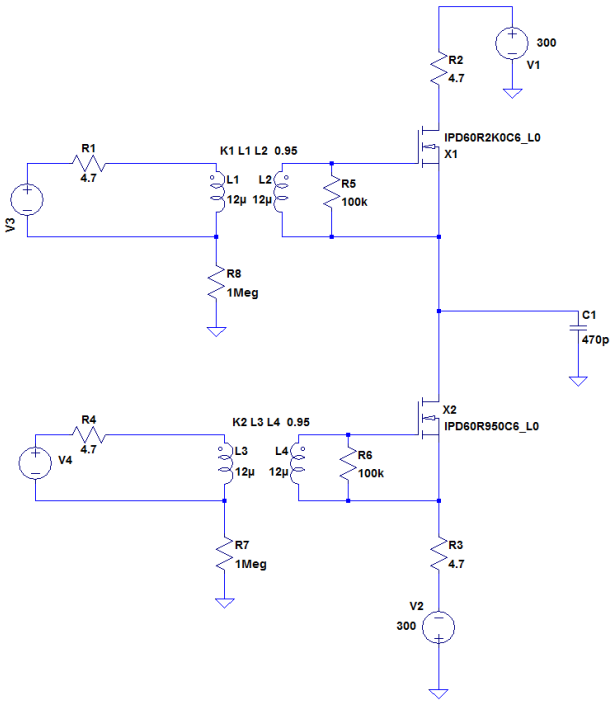

Fig. 4.2. Model used for transformer gate-drive topology simulation

The model for push-pull topology simulation is shown in (Fig. 4.3). This topology requires another custom transformer. For the porpoise of the simulation the values of the coils, like for transformer

gate drive topology, were measured from a DUT. Additionally, *RC* snubber circuits are used to mitigate oscillations occurring on the coils due to switching of the MOSFETs.

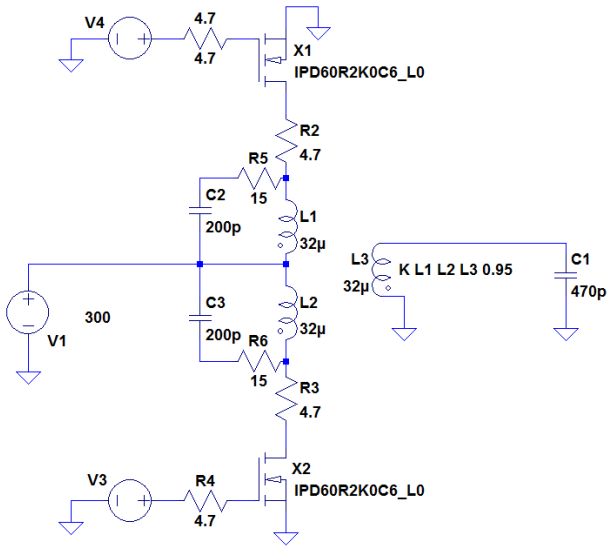

Fig. 4.3. Model used for push-pull topology simulation

The results of simulating the topologies are shown in (Table 4.2). Peak-to-average value is also present in the table, calculated using Formula (3.3). From this parameter a general view of the output waveform capabilities can be established. The closer the value is to 0 dB the better it represents a square wave.

Table 4.2. Results of simulating Si SJ and GaN transistors (10 MHz)

	IPD60R2K0C6				**GS-065-004**			
Half-bridge	V_{Mean}, V	V_{RMS}, V	V_{peak}, V	PAPR, dB	V_{Mean}, V	V_{RMS}, V	V_{peak}, V	PAPR, dB
Open (10 pF)	42.7	284.9	300	0.449	43.6	290.0	300	0.294
50 Ω	37.8	244.1	300	1.791	39.6	263.0	300	1.143
470 pF	45.9	232.2	300	2.225	39.9	271.1	300	0.880
1 nF	120.7	183.7	297	4.173	37.9	245.9	300	1.727
2 nF	133.0	166.9	279	4.463	42.2	193.8	288	3.441
Transformer gate	V_{Mean}, V	V_{RMS}, V	V_{peak}, V	PAPR, dB	V_{Mean}, V	V_{RMS}, V	V_{peak}, V	PAPR, dB
Open (10 pF)	32.5	290.0	300	0.294	36.5	292.1	300	0.232
50 Ω	19.3	251.0	300	1.549	12.8	267.0	300	1.012
470 pF	13.5	240.5	300	1.920	20.5	253.3	300	1.470
1 nF	-63.6	179.2	300	4.476	-40.1	221.0	288	2.300
2 nF	-66.1	174.9	296	4.570	-67.7	172.0	268	3.852
Push-pull	V_{Mean}, V	V_{RMS}, V	V_{peak}, V	PAPR, dB	V_{Mean}, V	V_{RMS}, V	V_{peak}, V	PAPR, dB
Open (10 pF)	0.0	246.7	366	3.426	1.0	273.6	430	3.927
50 Ω	0.0	211.1	304	3.168	1.6	231.0	342	3.408
470 pF	-0.4	254.8	410	4.132	0.0	296.0	420	3.039
1 nF	0.4	231.0	342	3.408	0.0	284.0	342	1.614
2 nF	-2.4	124.4	235	5.525	0.0	212.6	255	1.580

All three topologies are simulated using the models shown in (Fig. 4.1 - Fig. 4.3). From the time domain signal a clear difference can be observed for push-pull topology. Unlike half-bridge and transformer gate drive topologies, push-pull topology does not induce a DC component into the output signal, as can be indicated by the mean voltage (Table 4.2). While for the half-bridge and transformer gate drive topology an increasing mean voltage

Rise time is measured at conditions of 50 V and 1 MHz signal (Table 4.3). These conditions meet the conditions at which the rise time of topologies under test is measured. In the simulation the same two MOSFETs are tested.

Table 4.3. Rise times of topologies under test (50 V; 1 MHz)

	IPD60R2K0C6 (Si)			**GS-065-004 (GaN)**		
Load	Half-bridge	Transformer gate drive	Push-pull	Half-bridge	Transformer gate drive	Push-pull
Open (10pF)	12 ns	4.4 ns	17 ns	8.5 ns	1.4 ns	13 ns
50 Ω	12 ns	10 ns	20 ns	10 ns	9 ns	17 ns
470 pF	17 ns	14 ns	26 ns	14 ns	11 ns	22 ns
1 nF	28 ns	26 ns	49 ns	21 ns	18 ns	39 ns
2 nF	50 ns	44 ns	66 ns	36 ns	30 ns	55 ns

When comparing different topologies with the IPD60R2K0C6 MOSFET (Fig. 4.4), close results are observed between half-bridge and transformer gate driven topologies. In almost all case the difference in rise time is 2 to 6 nanoseconds. Rise times of push-pull topology are longer and are more than 10 ns in difference when compared with previously discussed topologies. When the eGaN FET is in question, obviously faster rise times can be seen. And as is in the case with Si MOSFET, the push-pull topology produces the longest rise times. Both half-bridge and transformer gate drive topology show improved and similar rise times. From the simulation results and taking into the account the rise time of the topologies under test, half-bridge and transformer gate drive topologies show the most potential for achieving the highest signal frequencies.

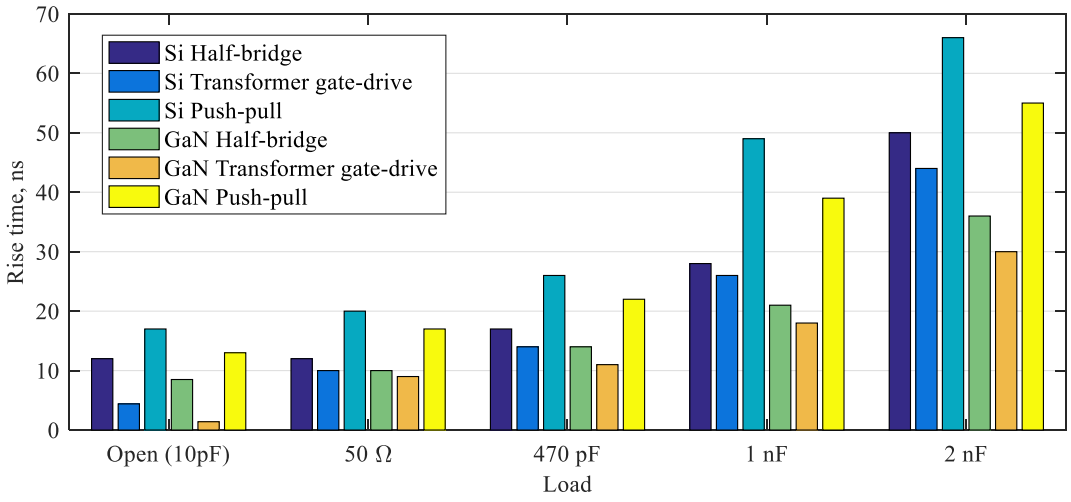

Fig. 4.4. Rise times of topologies under test with Si and GaN transistors at different loads

4.2. Preparations for taking measurements

To take measurements to evaluate different pulser topologies, an automated test stand was set up (Fig. 4.5) using available instruments at the laboratory of the university. A *Python* programming language script was written to send commands from the computer to the instruments and collect the measured data from the oscilloscope. Instruments and other equipment used for this purpose are listed below:

- Rigol DS4034 oscilloscope (350 MHz; 4 GSa/s);
- Siglent SDG6022X pulse/arbitrary waveform generator (200 MHz; 2.4 GSa/s);
- MCP M10-QP305 DC power supply (0-30 V; 0-5 A);
- MCP M10-OPP300 high voltage DC power supply (0-300 V; 0-0.4 A);

The measurement setup is shown in (Fig. 4.5). The device under test (DUT) is highlighted in yellow.

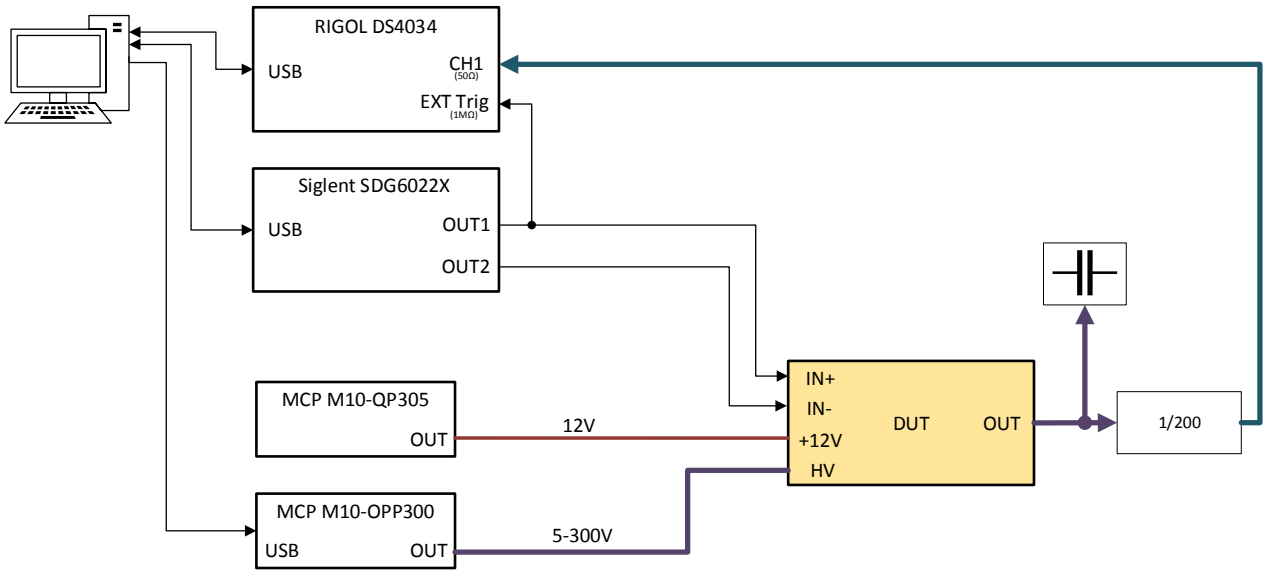

Fig. 4.5. Setup of the experiment for measuring output signal of the topologies

The generator doe, with s a burst of 10 pulses in both output channels, but the second channel is offset by 180°. The generator is triggered by a manual trigger via USB interface, while the oscilloscope trigger is activated by the output signal of the generator. The pulser output is loaded with the capacitive or 50 Ω resistive load. The output signal is also fed into a 1/200 divider with a 50 Ω output impedance which is connected to the input of the oscilloscope set for 50 Ω impedance. The high voltage power supply is controlled by the PC and the voltage value is set by a command. The full automation of the test allows for thorough investigation of the pulsers. The collected data is further processed with MATLAB.

The frequency of the generator is increased from 1 MHz to 35 MHz in 1 MHz increments. The voltage of HV is picked to represent pseudo logarithmic value grid: 5, 10, 15, 20, 25, 30, 40, 50, 75, 100, 125, 150, 200, 250 and 300 volts. The experiment is repeated four times with different valued loads. The sweep of both voltage and frequency allows to gather more information of the full output capabilities of the pulser.

4.3. Measurement results of the high voltage pulsers

Each of the high voltage pulser is loaded with 4 different loads: 50 Ω, 470 pF, 1 nF and 2 nF. The pure capacitive loads are chosen over a real ultrasonic transducer to simplify testing and to evaluate full pulser output signal generation capabilities. In many cases ultrasonic transducers are narrow banded devices with their specifically designed centre frequency. This would prevent the full bandwidth of the pulser to be discovered. As ultrasonic transducers act mainly as a capacitive load, the use of only this component in testing can be justified instead of a complex load, as described in the *Butterworth-Van Dyke* model.

4.3.1. Half-bridge topology

Half-bridge topology, and others assessed in this part, use the IPD60R2K0C6 super-junction MOSFET as the main switch. In all three cases, the switch element is identical and only the nature of the circuitry is in question. And as well as in simulation models discussed in previous chapter, in the circuits under test, 4.7 Ω value resistors are used on the high voltage rails. These resistors help to limit the current and reduce the voltage transient over the MOSFET, keeping the circuit stable and avoiding breakdown. By using four different loads, frequency response is found using SWC (Fig. 4.6).

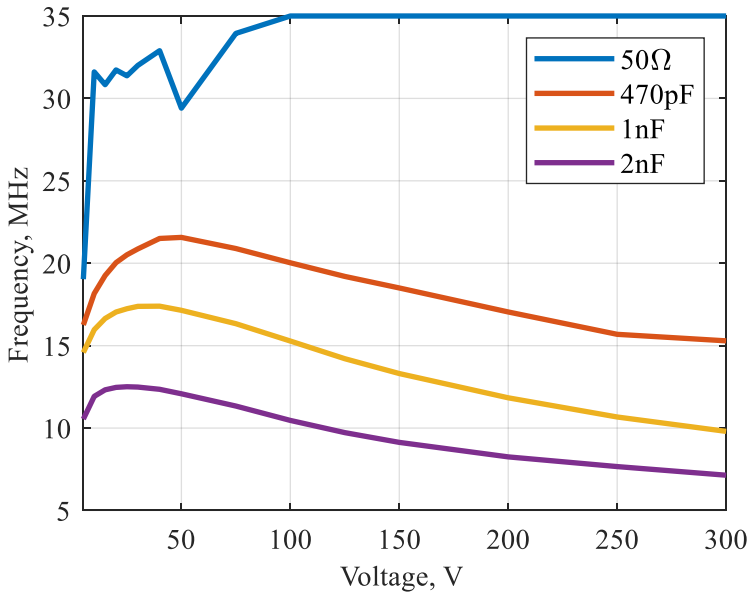

Fig. 4.6. Cut-off frequency of half-bridge topology found by SWC result

From (Fig. 4.6) the maximum frequency with each load can be observed. The peak frequency of 21.7 MHz is achieved at 50 V for the 470 pF load and with increasing capacitive load the peak frequency is achieved with lower voltage on the output stage. The lowest achievable frequency is at the maximum high voltage supply value, which is 7.2 MHz for the 2 nF load at 300 V. By using a purely resistive load of 50 Ω a maximum frequency of 35 MHz can be achieved beyond 100 V output level.

The three main variables that determine the output signal of the pulser are: excitation frequency, voltage of the output stage and load. To make the experiments shorter, the loads are kept to a minimum sample size of 4 with values of: 50 Ω, 470 pF, 1 nF and 2 nF. The frequency and the output

voltage are changed incrementally with all different loads and full output level maps are found (Fig. 4.7). The contour maps are divided in 3 dB increments, where the 0 dB reference voltage is set to the set voltage bus of the output stage. Value of each contour line is marked on the map. From these maps the full working range of the pulser can be found when loaded with different loads.

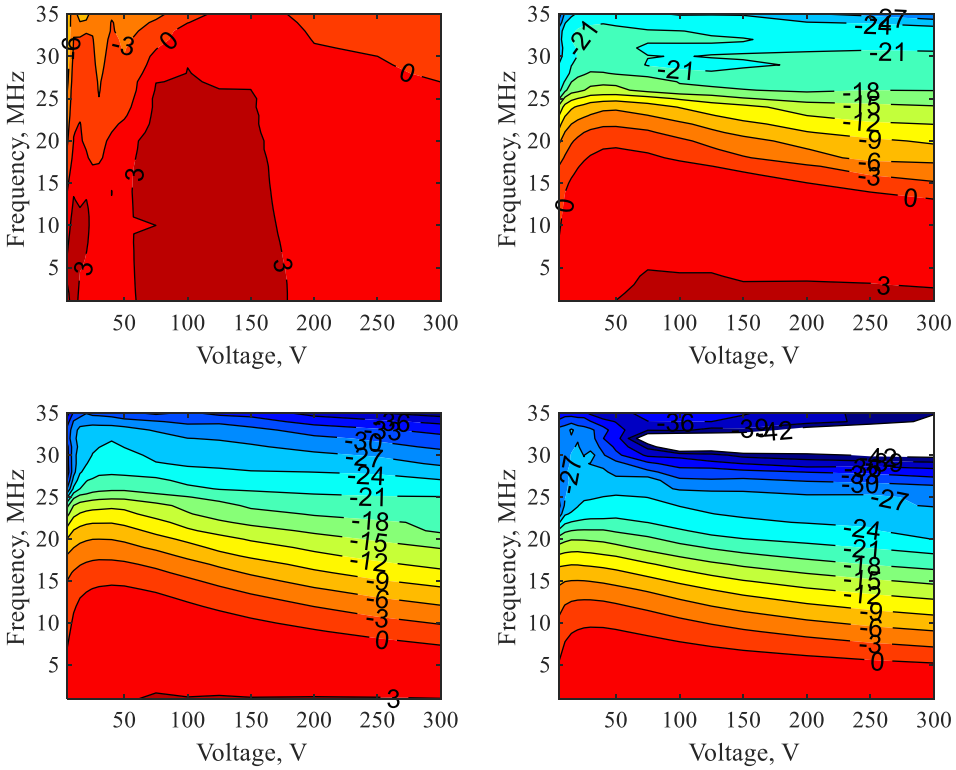

Fig. 4.7. Output of the half-bridge topology with 50 Ω load (top left), 470 pF load (top right), 1 nF load (bottom left) and 2 nF load (bottom right)

For more in-depth view of the output levels of the half-bridge topology contour plots are shown (Fig. 4.7), loaded with a 50 Ω resistive load and three different value capacitors. The usable range of the pulser (down to -3 dB mark) are clearly indicated by the graph. As indicated by (Fig. 4.6) the widest bandwidth is achieved with a resistive load. This is also visible by the plot (Fig. 4.7), but the resistive load output has the steepest decline of signal amplitude below the -3 dB boundary. From the plot of 470 pF load it can be deducted, that even though in higher voltage range (above 100 V) maximum achievable frequency is lower than that in the lower voltage range. But for the low frequencies (below 5 MHz) a maxima area is observed from 100 V to 300 V range.

The maximum output frequency is also determined by the rise time of the signal. In this case a 1 MHz signal is analysed, and the rise time is found (Fig. 4.8). By using (3.2) formula, a maximum output frequency can be estimated (Fig. 4.9) from the rise time.

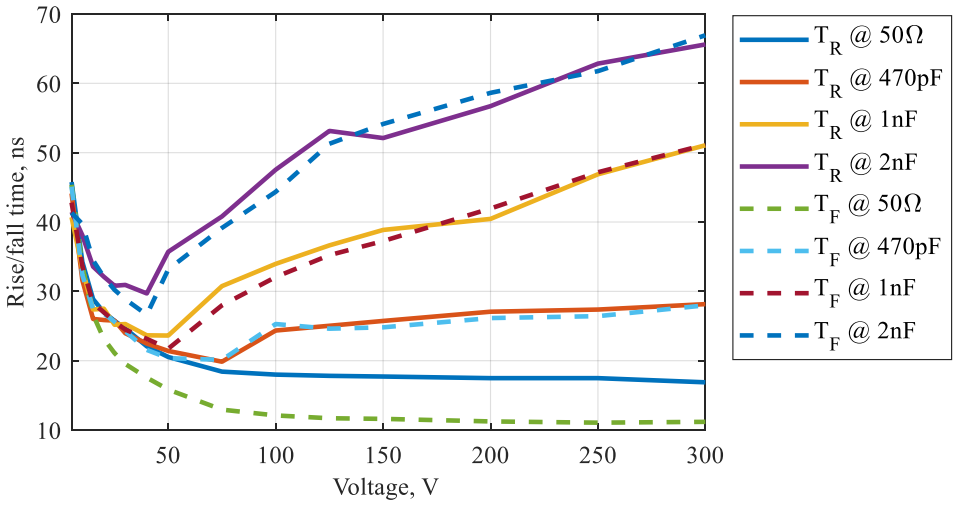

Fig. 4.8. Rise and fall times of 1 MHz signal in half-bridge topology

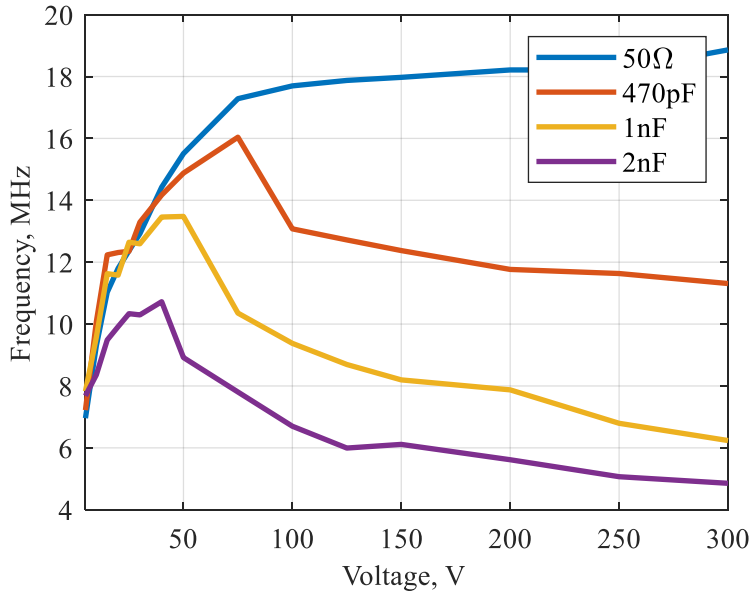

Fig. 4.9. Cut-off frequency of half-bridge topology derived from signal rise time at 1 MHz

When observing the rise time of the 50 Ω load, the absence of the output capacitance is clearly seen. This is in accordance with the lower output capacitance of the MOSFET, with an increase of the drain-source voltage the capacitance drops and rise time shortens. When the pulser is loaded with a capacitive lad, the decrease of the output capacitance of the MOSFET only has an effect until a certain point, after that the capacitive load becomes the dominant part and the rise time increases. When comparing the cut-off frequency and the maximum frequency derived from the rise times a similarity is observed. For all capacitive loads, the frequency curves share similar frequency values and the maximum value drift.

The correlation results between the measured signal and an ideal signal are shown below (Fig. 4.10). On the graph on the left, it is observed that the signal of the 50 Ω load presents the lowest value of correlation amongst all the capacitive loads. This can be explained by looking at the time domain of

the captured signals. When comparing only the capacitive loads, better correlation results are observed for lower capacitance loads. This difference is clearly shown at the 200 V signal, where the loads (470 pF, 1 nF, 2 nF) cross the 0.8 mark at 14.5 MHz, 12 MHz, and 8 MHz, and the 0.7 mark at 16 MHz, 13 MHz, and 10 MHz, respectively.

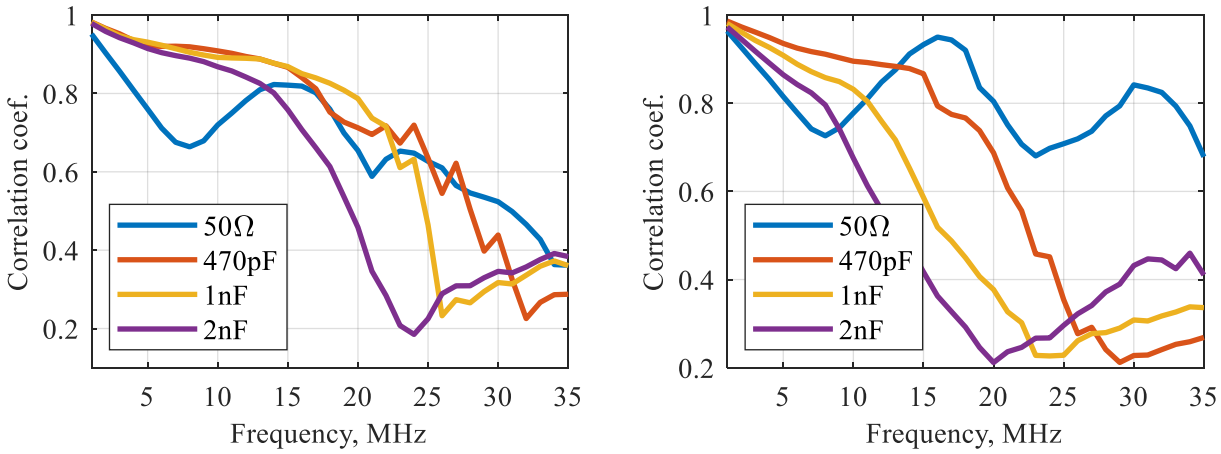

Fig. 4.10. Correlation results at 50 V (left) and 200 V (right) for half-bridge topology

Time domain signals are shown in (Fig. 4.11). Observations are made at 16 MHz and 20 MHz frequencies at 200 V on the output and 470 pF load. These frequencies represent the close values of cut-off frequencies found by correlation with square wave (Fig. 4.10 (right)) at 0.7 and 0.8 threshold.

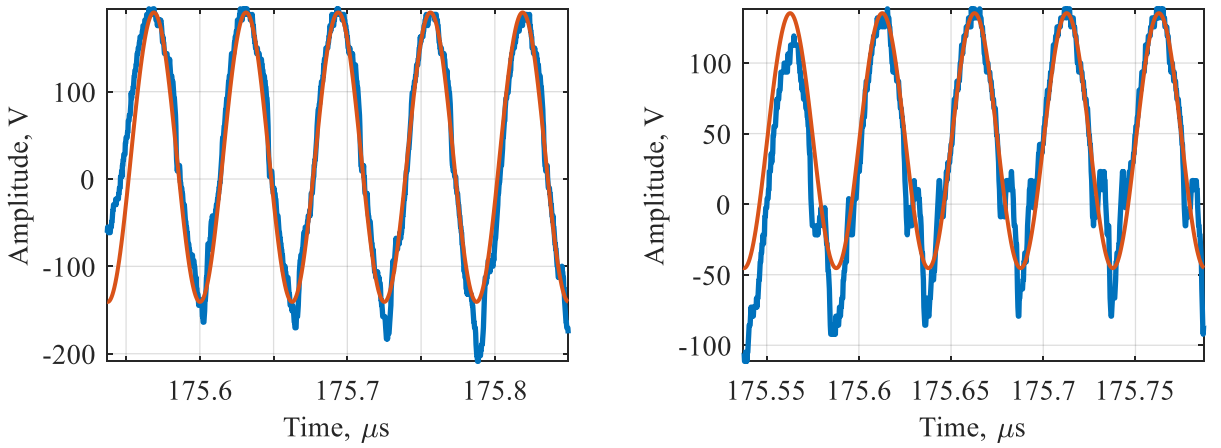

Fig. 4.11. Half-bridge pulser output of 16 MHz (left) and 20 MHz (right) signals (blue) and fitted SWC results (orange) at 200 V and 470 pF load

The time difference between a set pulse width (half the time of the set period), and a measured pulse width is shown below (Fig. 4.12). The measurement was done on the positive pulse. Firstly, when the output voltage is increased the lower maximum achievable frequency is observed, just as from the frequency response graph (Fig. 4.6). As expected, the higher the load capacitance the bigger distortions occur, meaning the signal is not symmetrical and does not represent wanted output waveform.

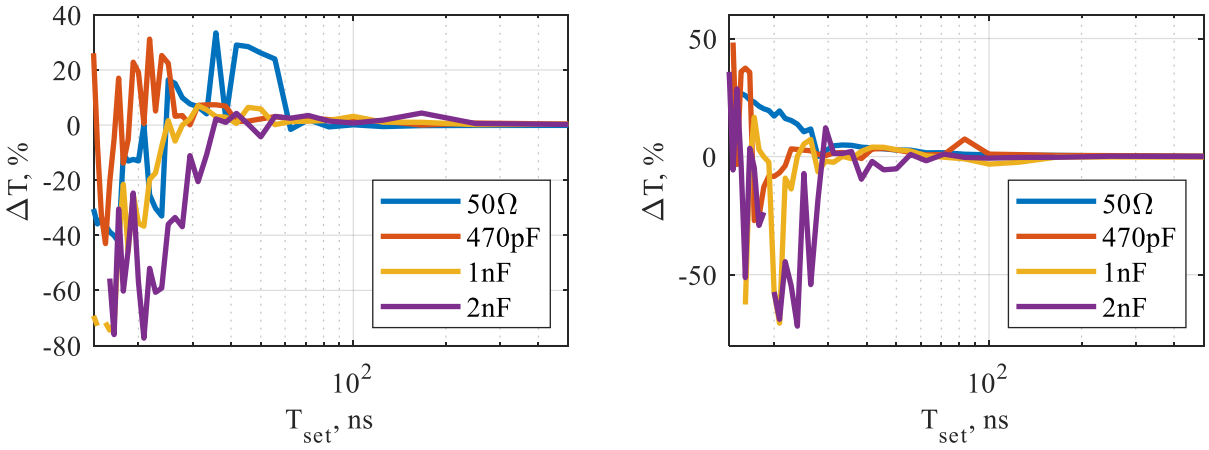

Fig. 4.12. Time difference vs set pulse width for half-bridge topology at 50 V (left) and 200 V (right)

The time differences are shown at two output voltages. As seen from the cut-off frequency curve (Fig. 4.6) the maximum frequency decreases as the voltage increases. This also can be observed from the pulse width (Fig. 4.12). The time difference between set and measured pulse width begins to increase at lower frequencies when the voltage increases. In all four cases the 50 Ω load shows almost identical time difference over set period and it reaches the 10 % difference at 50 ÷ 60 ns (10 MHz ÷ 8.3 MHz). For the 470 pF load at 50 V the time difference of less than 10 % can be observed down to 15 ns set pulse width (33.3 MHz). For 1 nF and 2 nF loads the maximum frequency, below 10 % increase in time difference, are 13 ns (38.4 MHz) and 22 ns (22.7 MHz) equivalently.

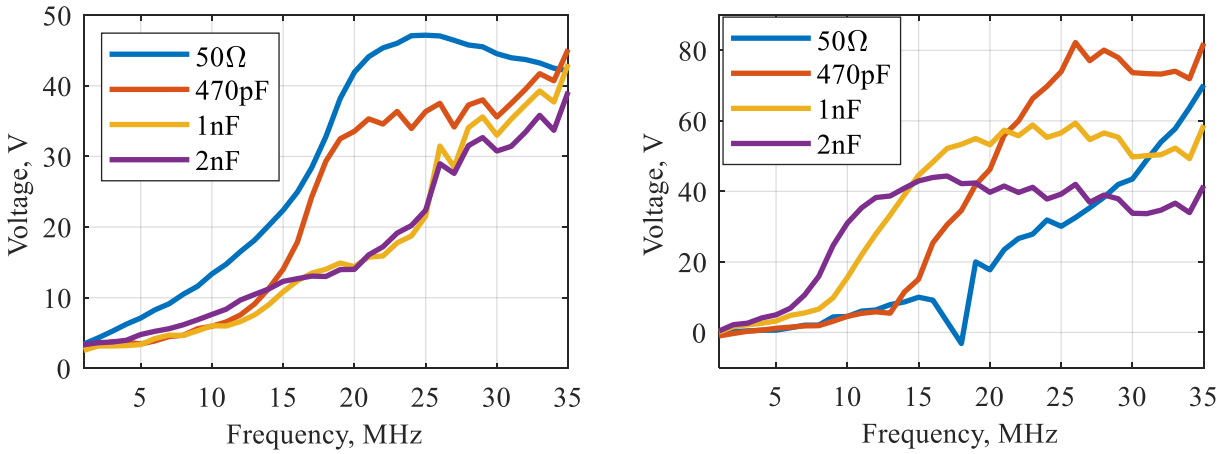

Fig. 4.13. DC offset in the measured signal for half-bridge topology at 50 V (left) and 200 V (right)

Another parameter that can be helpful to evaluate different topologies is DC offset, as notable voltage drift is observed when frequency of the output is increased. This DC voltage offset vs frequency graph is shown in (Fig. 4.13) at 50 V and 200 V output voltages.

4.3.2. Transformer gate drive topology

By using four different loads, frequency response is found by using SWC (Fig. 4.14). When observing the cut-off frequency, a peak value for the capacitive loads is observed at 30 V and it reaches 29.1 MHz. For the 50 Ω load, a slight peak can be interpreted at 200 V, but despite the slight dip at

30 V, it is similar to a pure resistive load observed at half-bridge topology. The lowest achievable frequency is at the maximum high voltage supply value, which is 7.5 MHz for the 2 nF load at 300 V. By using a purely resistive load of 50 Ω a maximum frequency of 32.0 MHz can be achieved at 200 V output level.

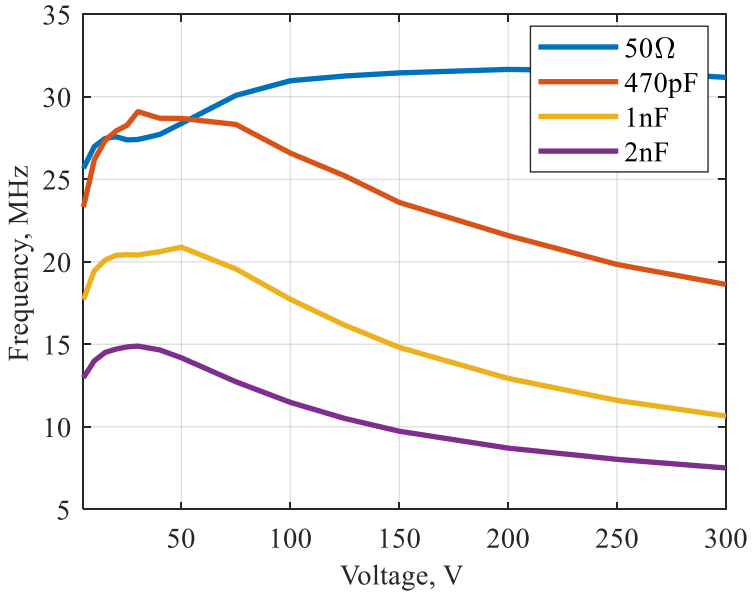

Fig. 4.14. Cut-off frequency of transformer gate-drive topology found by SWC result

A more in-depth view of the output levels of the transformer gate-drive topology contour plots are shown (Fig. 4.15), loaded with a 50 Ω resistive load and three different value capacitors. A major difference with half-bridge topology is noticeable on the resistive load. While half-bridge topology had a steep decline with 50 Ω load, transformer gate drive topology does not show this attribute and presents a much milder amplitude decline below the -3 dB mark. For the capacitive loads, it is very similar case to the half-bridge topology, but with only the amplitude of the signal being greater. In all cases a 3 dB amplitude is observed at the lower frequency range.

The maximum output frequency is also determined by the rise time of the signal. In this case a 1 MHz signal is analysed and rise time for each voltage step is found (Fig. 4.16). From the rise time, using (3.2) expression, a maximum output frequency can be estimated (Fig. 4.17).

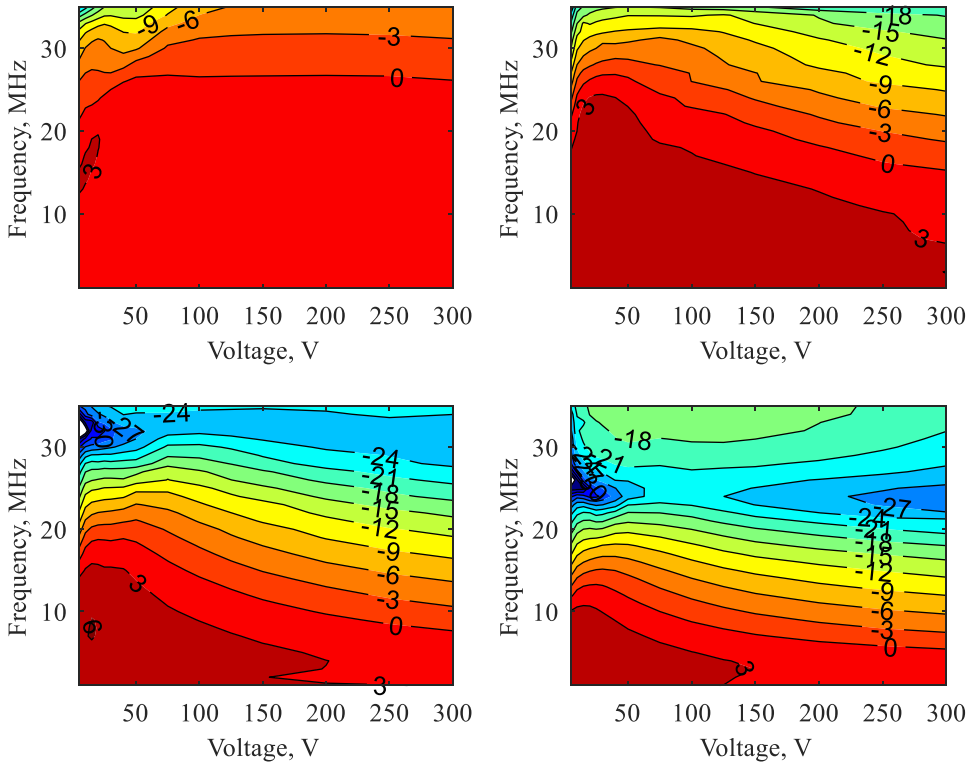

Fig. 4.15. Output of the transformer gate-drive topology with 50 Ω load (top left), 470 pF load (top right), 1 nF load (bottom left) and 2 nF load (bottom right)

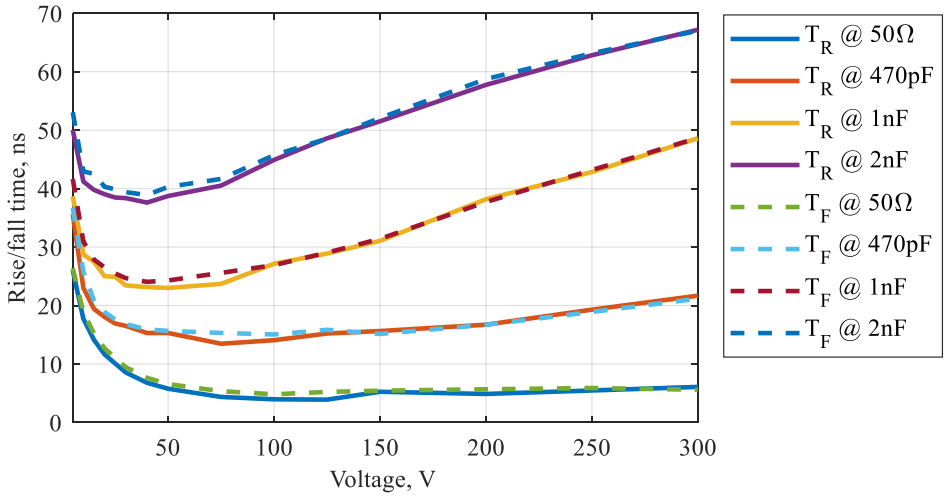

Fig. 4.16. Rise and fall times of 1 MHz signal in transformer gate-drive topology

When comparing the rise time and the maximum frequency derived from it, the maximum frequency drift is notable, which was not detected from the cut-off frequency graph. When compared with half-bridge topology the rise times for each load a difference can be seen for the 50 Ω load. When considering the capacitive loads, a slight improvement can be detected. For the 470 pF load a difference of 5 MHz is present when compared with half-bridge topology. And for the 2 nF load a decrease of 1 MHz is observed at 50 V mark and an increase of 2 MHz at 300 V mark.

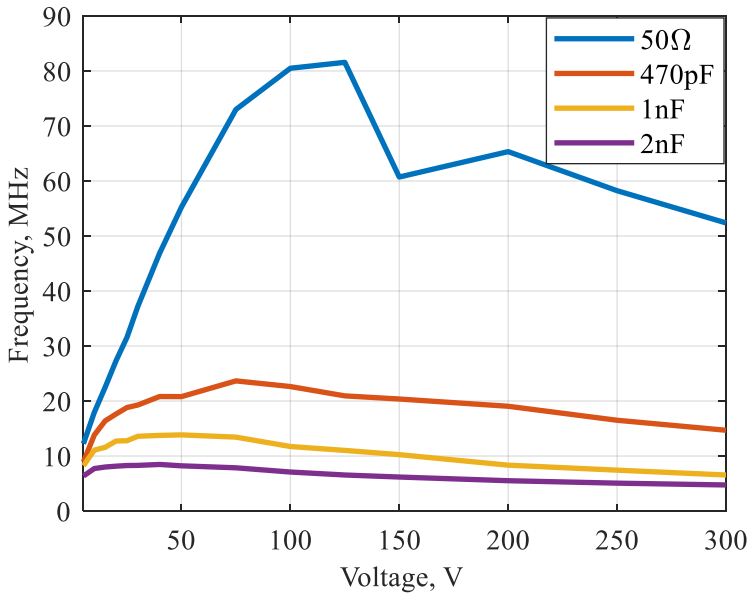

Fig. 4.17. Cut-off frequency of transformer gate-drive topology derived from signal rise time at 1 MHz

The correlation results between the measured signal and an ideal signal are shown below (Fig. 4.18). On the graph on the left, it is observed that the signal of the 50 Ω load presents the lowest value of correlation amongst all the capacitive loads up to roughly 20 MHz, after which an increase can be seen. This can be explained by looking at the time domain of the captured signals. When comparing only the capacitive loads, better correlation results are observed for lower capacitance loads, where the loads (470 pF, 1 nF, 2 nF) cross the 0.8 mark at 17 MHz, 19.5 MHz and 14 MHz, and the 0.7 mark at 21 MHz, 22 MHz and 16 MHz respectively, with 50 V on the output.

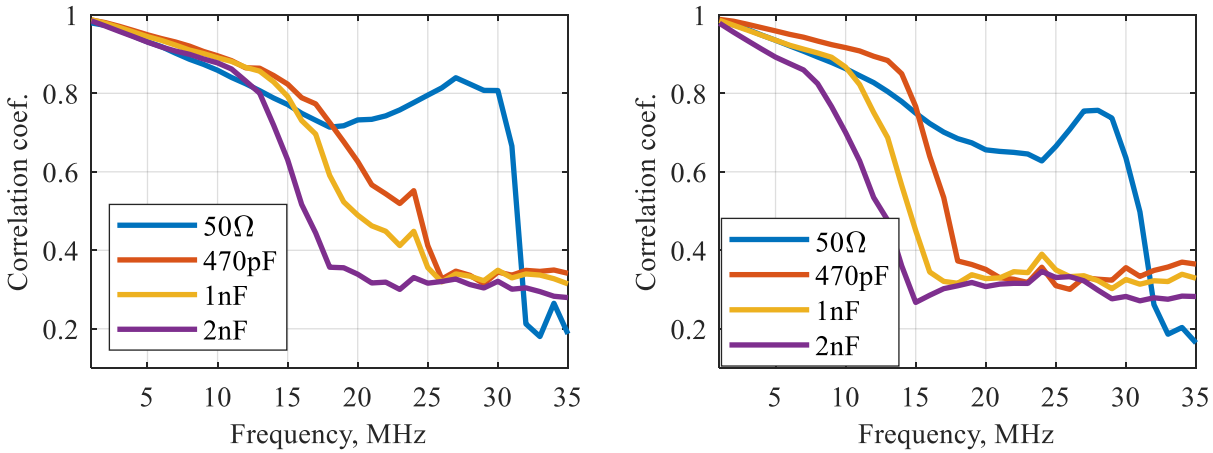

Fig. 4.18. Correlation results at 50 V (left) and 200 V (right) for transformer gate-drive topology

To observe time domain (Fig. 4.19) signal decline with 470 pF load at 200 V, 14 MHz and 16 MHz signals are chosen, as they represent the 0.7 and 0.8 correlation result values.

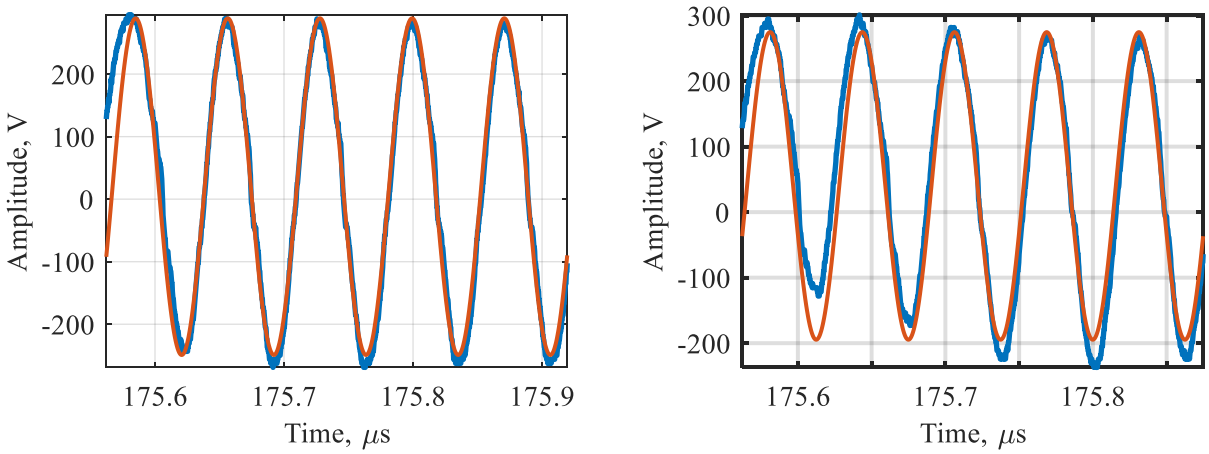

Fig. 4.19. Transformer gate-drive pulser output of 14 MHz (left) and 16 MHz (right) signals (blue) and fitted SWC results (orange) at 200 V and 470 pF load

The time differences are shown at two output voltages (Fig. 4.20). As seen from the cut-off frequency curve (Fig. 4.14) the maximum frequency decreases as the voltage increases. The time difference between set and measured pulse width begins to increase at lower frequencies when the voltage increases. In all cases the 50 Ω load shows almost identical time difference over set period and it reaches the 10 % difference at 18 ns (27.7 MHz). For the 470 pF load at 50 V the time difference of less than 10 % can be observed down to 20 ns set pulse width (25 MHz). For 1 nF and 2 nF loads the maximum frequency below 10% increase in time difference are 26 ns (18 MHz) and 50 ns (10.0 MHz) equivalently.

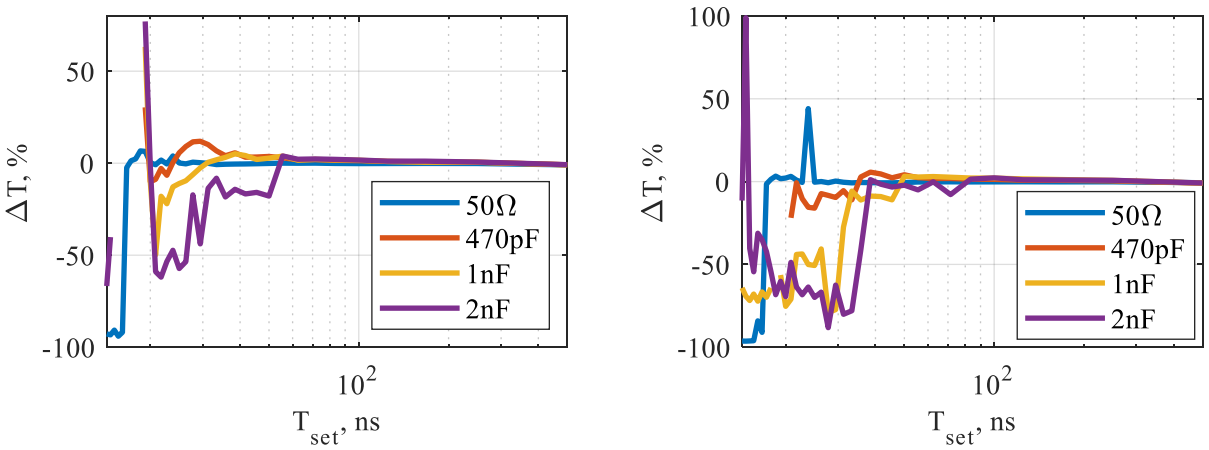

Fig. 4.20. Time difference vs set pulse width for transformer gate-drive topology at 50 V (left) and 200 V (right)

Another parameter that can be helpful to evaluate different topologies is DC offset, as notable voltage drift is observed when frequency of the output is increased. This DC voltage offset vs frequency graph is shown in (Fig. 4.21) at 50 V and 200 V output voltages.

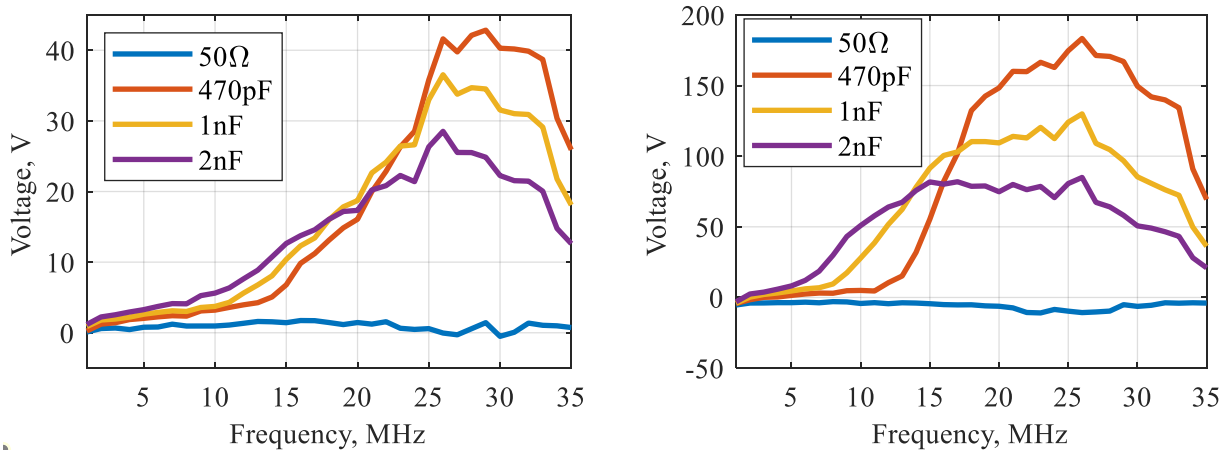

Fig. 4.21. DC offset in the measured signal for transformer gate-drive topology at 50 V output (left) and 200 V output (right)

4.3.3. Push-pull output topology

By using four different loads, frequency response is found by using SWC (Fig. 4.22). When observing the cut-off frequency, a peak value for the capacitive loads is observed at 20 V and it reaches 16.8 MHz for 1 nF load and 12.2 for 2 nF load. When loaded with 470 pF capacitance, a peak at 50 V of 26.3 MHz is observed. For the 50 Ω load, the boundary for the automated testing was set for 35 MHz and it did not reach the maximum output frequency capability of the pulser. The lowest achievable frequency is at the maximum high voltage supply value, which is 7.8 MHz for the 2 nF load at 300 V and 20.5 MHz for the 470 pF load at 300 V.

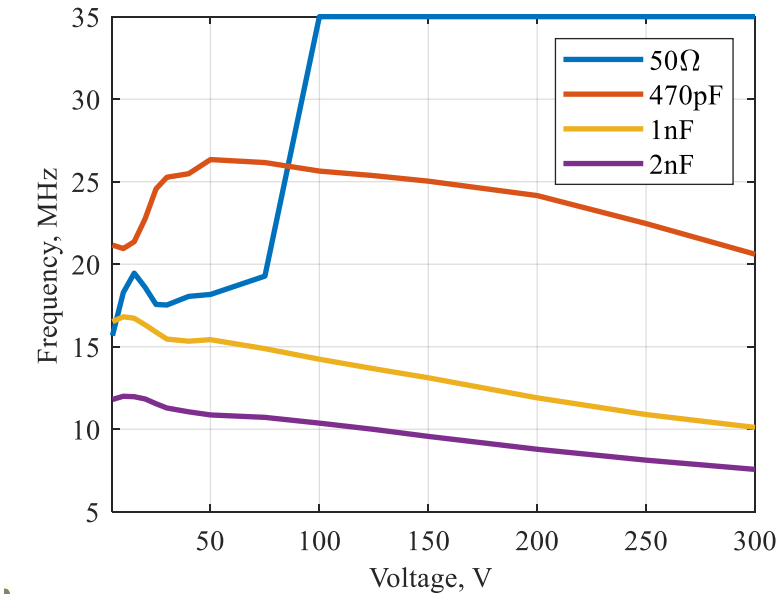

Fig. 4.22. Cut-off frequency of push-pull topology found by SWC result

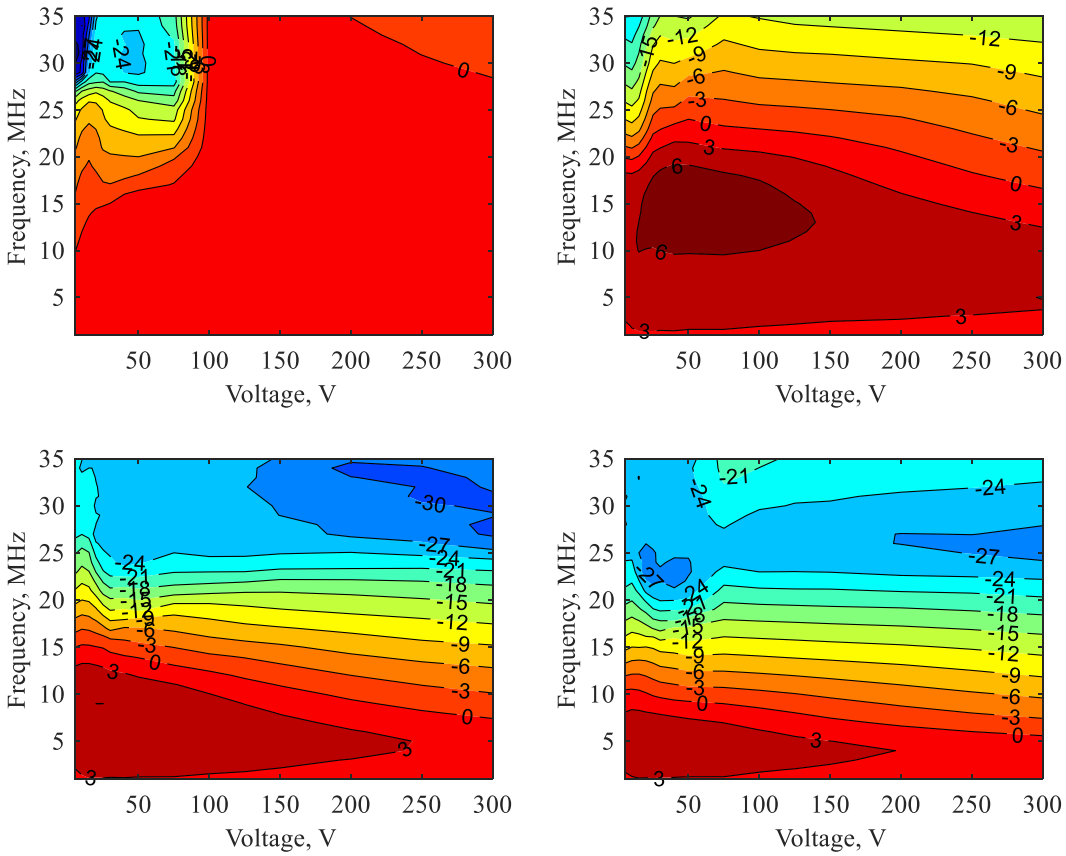

Fig. 4.23. Output of push-pull topology with 50 Ω load (top left), 470 pF load (top right), 1 nF load (bottom left) and 2 nF load (bottom right)

A more in-depth view of the output levels of the half-bridge topology contour plots are shown (Fig. 4.23), loaded with a 50 Ω resistive load and three different value capacitors. When compared to half-bridge and transformer gate drive topologies, a clear difference is observed regarding the output signal of the pulser. Push-pull topology presents a slight resonance on the output stage. The peak value is changing, depending on the load capacitance: with 470 pF the peak is at 14 MHz, with 1 nF load it is at 9 MHz, and with 2 nF load is at 5 MHz. With a resistive load it is notable that the pulser is performing well with higher than 100 V voltages. For low capacitance loads (470 pF) it is notable the shallow decline of the amplitude below the -3 dB boundary.

The maximum output frequency is also determined by the rise time of the signal. In this case a 1 MHz signal is analysed and rise time for each frequency step is found (Fig. 4.24). From the rise time, using (3.2) expression, a maximum output frequency can be estimated (Fig. 4.25).

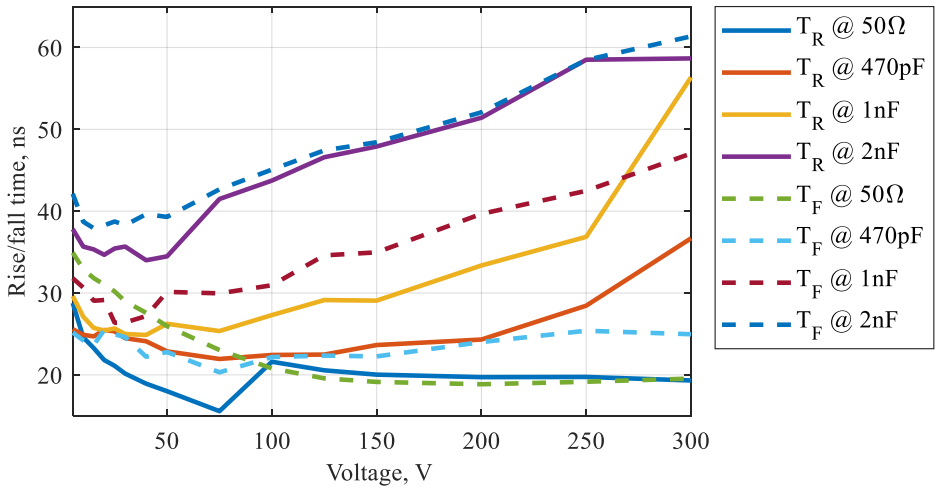

Fig. 4.24. Rise and fall times of 1MHz signal in push-pull topology

When comparing the rise time and the maximum frequency derived from it, the maximum frequency is lower than the frequency found by applying SWC to the output signal. When compared with half-bridge and transformer gate drive topologies the rise times for each load are considerably longer. This can be explained by the nature of push-pull topology, which forms an *RLC* circuit on the output stage.

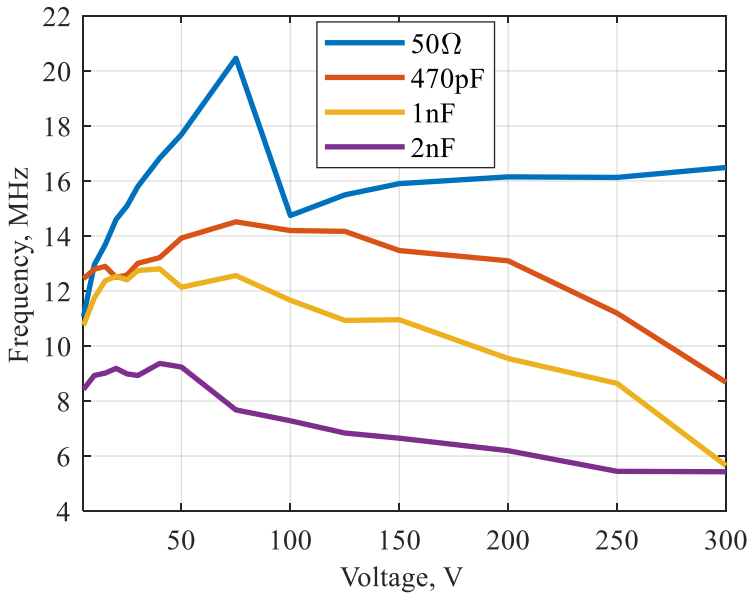

Fig. 4.25. Cut-off frequency of push-pull topology derived from signal rise time at 1 MHz

The correlation results between the measured signal and an ideal signal are shown below (Fig. 4.26). For the push-pull topology, the correlation does not represent the actual performance of the output of the pulser. In the best case the correlation with an ideal signal does not produce a value above 0.75. This can be explained by the *RLC* circuit present in the output stage. It does not only act as a filter but at 15 MHz, with a 470 pF load and 50 V ÷ 100 V on the output, a resonance occurs. Both filtered signal and an increase in amplitude due to the resonance diverge from an expected ideal square wave signal, making the correlation result low in value.

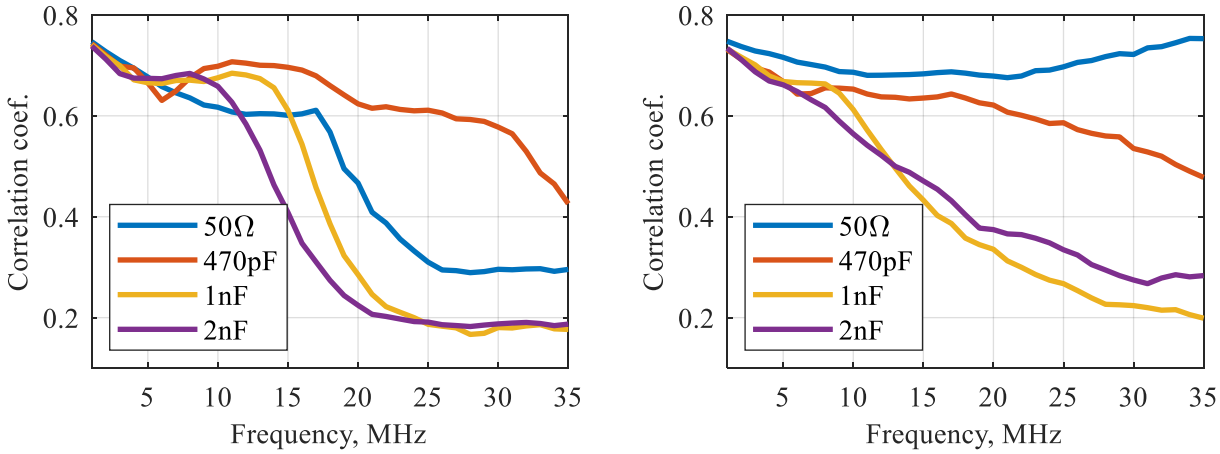

Fig. 4.26. Correlation results at 50 V (left) and 200 V (right) for push-pull topology

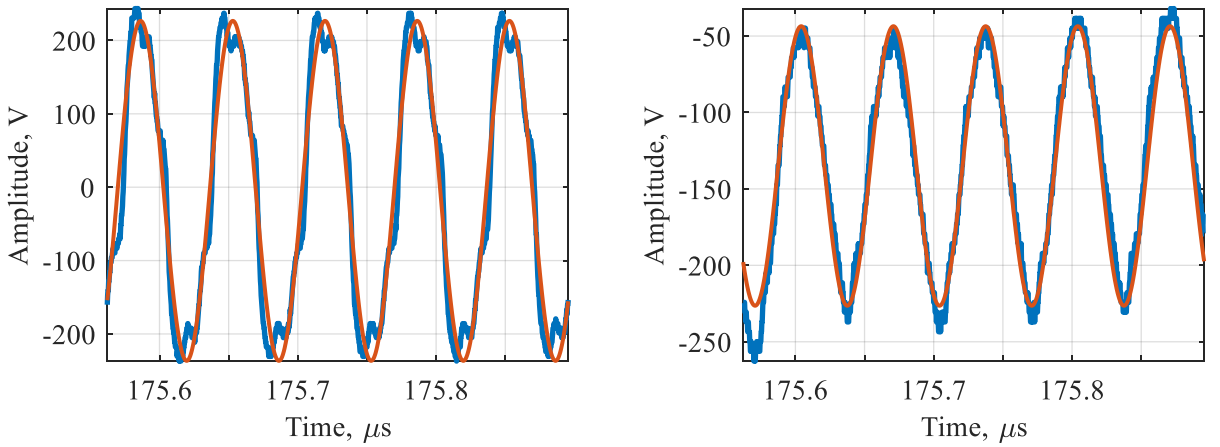

Fig. 4.27. Push-pull pulser output of 15 MHz frequency signal (blue) and fitted SWC results (orange) at 200 V and with 50 Ω (left) and 1 nF load (left)

The time differences are shown in (Fig. 4.28). When the pulser is loaded with 50 Ω load and 300 V are on the output very little time difference can be excelled throughout the whole frequency range. In all four cases the 50 Ω load shows almost identical time difference over set period and it reaches the 10 % difference at 50 ÷ 60 ns (10 MHz ÷ 8.3 MHz). For the 470 pF load at 50 V the time difference of less than 10 % can be observed down to 15 ns set pulse width (33.3 MHz). For 1 nF and 2 nF loads the maximum frequency below 10 % increase in time difference are 13 ns (38.4 MHz) and 22 ns (22.7 MHz) equivalently.

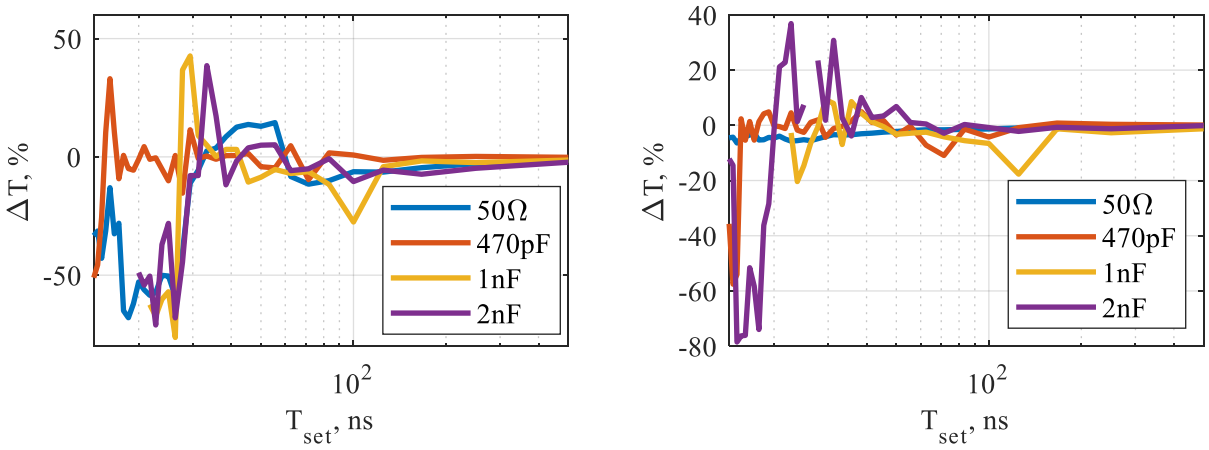

Fig. 4.28. Time difference vs set pulse width for push-pull topology at 50 V (left) and 200 V (right)

Another parameter that can be helpful to evaluate different topologies is DC offset, as notable signal drift is observed when frequency of the output is increased. This DC voltage offset vs frequency graph is shown in (Fig. 4.29) at 50 V and 200 V output voltages.

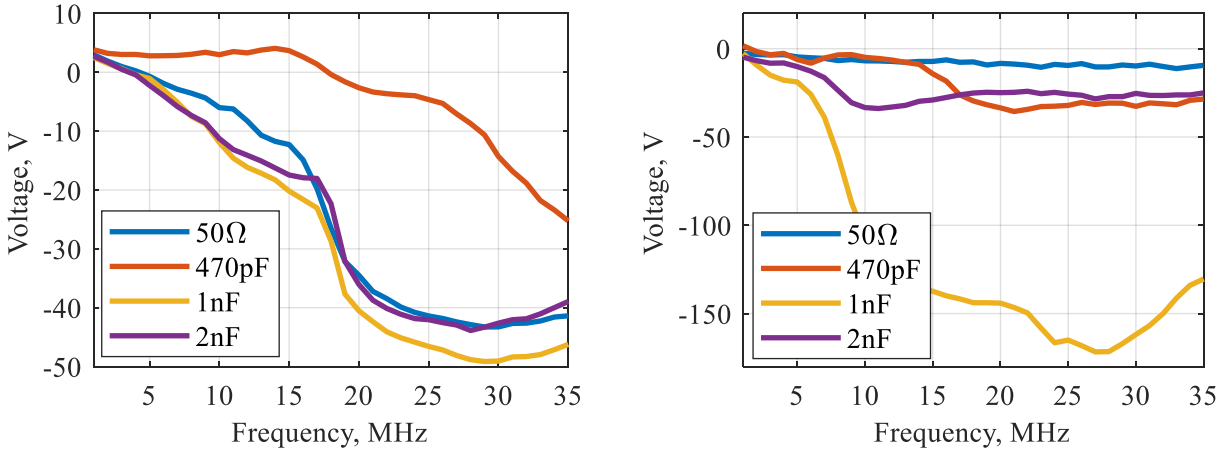

Fig. 4.29. DC offset in the measured signal for push-pull topology at 50 V (left) and 200 V (right)

4.4. Determining the best candidate for further investigation

For every method tested, the maximum output frequency is found (Table 4.4). All different methods in evaluating maximum frequency can be compared with the results found by sine wave correlation. Rise time measurements with 1 MHz signal show results falling short of the actual cut-off frequency. Time difference between set and actual pulse width is an informative metric about the quality of the output signal, although determining the cut-off frequency is unreliable. The most promising results are shown by correlation with an ideal square wave. This method closely resembles SWC but instead of a harmonic signal, a square wave is used. This square wave represents a set output signal which is expected on the output of the pulser. In the case for transformer gate-drive topology, this method showed good results and the correlation result between 0.7 and 0.8 closely resemble the output cut-oof frequency found with correlation with a harmonic signal. But in the case for the push-pull topology, which is prone to having resonance occur on the output stage, thus leading to amplitude increases above the nominal value, the correlation with an ideal waveform does not represent the

actual output capabilities of the pulser. The correlation will always provide a low value (usually below 0.8) and for the push-pull topology correlation as a method for determining the maximum output frequency becomes unusable.

Table 4.4. Maximum frequencies of topologies under test

Topology	Load	f_{max} (SWC), MHz	f_{max} (t_{rise}), MHz	f_{max} (ΔT), MHz	f_{max} (Corr. (0.8)), MHz	f_{max} (Corr. (0.7)), MHz
Half-bridge	50Ω	35.0	19.0	12.0	11.0	14.0
	470pF	21.7	16.0	22.0	14.5	16.0
	1nF	17.2	13.5	24.0	12.0	13.0
	2nF	12.8	11.0	15.0	8.0	10.0
Transformer gate drive	50Ω	32.0	80.0	33.0	13.0	32.0
	470pF	29.1	24.0	16.0	17.5	22.0
	1nF	20.7	14.0	18.0	19.0	23.0
	2nF	15.0	9.0	10.0	14.0	16.0
Push-pull	50Ω	35.0	20.0	35.0	N/A	N/A
	470pF	26.3	14.5	33.0	N/A	N/A
	1nF	16.8	13.0	18.0	N/A	N/A
	2nF	12.2	9.0	15.0	N/A	N/A

For all topologies and loads with a 10 MHz signal and 300 V on the output stage, PAPR is calculated (Table 4.5) using Formula (3.3). A comparison with simulated results is made (Fig. 4.30). Measured results show much higher PAPR values, but that is to be expected, as simulation was done for an ideal case where only gate driver, transistor, current limiting resistor, and the load were the only variables. In real case a lot more parasitic components are present in the circuit, such as, inductance and resistance of the PCB traces, parasitic capacitance, also protection diodes are used in a real pulser.

Table 4.5. Calculated PAPR values of topologies under test

Topology	Load	V_{PEAK}, V	V_{RMS}, V	PAPR, dB
Half-bridge	50 Ω	305.44	271.04	1.038
	470 pF	380.77	272.67	2.900
	1 nF	300.27	149.87	6.035
	2 nF	205.32	92.71	6.905
Transformer gate-drive	50 Ω	342.34	266.83	1.695
	470 pF	437.01	293.02	3.501
	1 nF	289.64	167.15	4.774
	2 nF	229.57	105.47	6.755
Push-pull	50 Ω	345.05	252.56	2.710
	470 pF	515.98	345.11	3.493
	1 nF	351.64	158.97	6.894
	2 nF	293.88	118.37	7.898

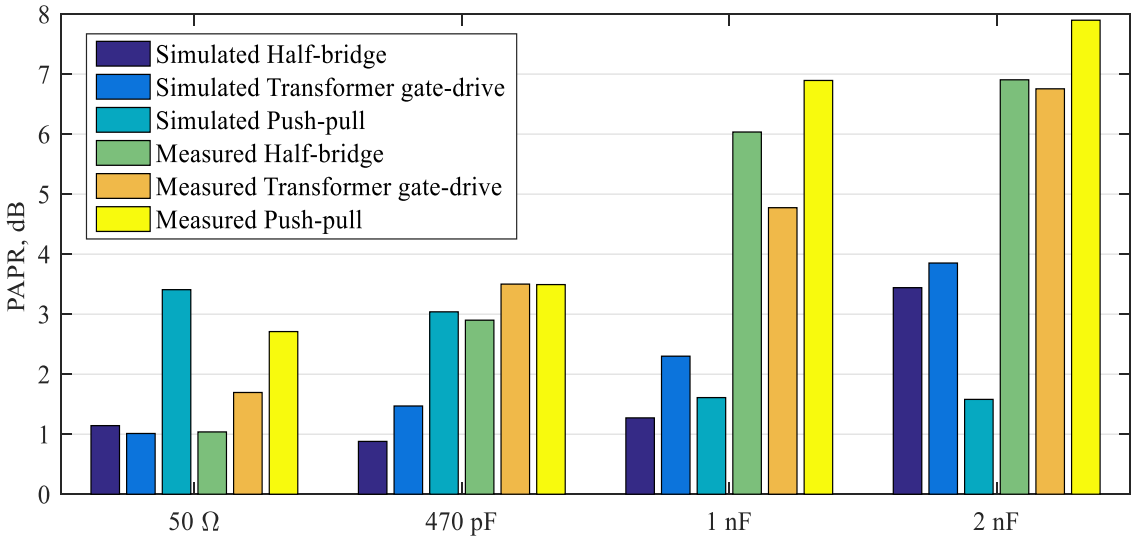

Fig. 4.30. Comparison of measured and simulated results of PAPR

For the key points of maximum frequency determined by SWC, a sample size of 10 is collected, and standard deviation of output voltage level is found (Table 4.6). The maximum frequency point is found using linear interpolation on cut-off frequency data of the pulsers. The best and worst cases, which are 50 Ω and 2 nF loads are investigated. In all cases a stable output voltage is found at each of the key points, indicated by relatively low standard deviation. For example, in the case of half-bridge topology loaded with 2 nF load and 25 V set on the output stage, the average output voltage at the cut-off frequency was found to be 17.58 V, with a standard deviation of 0.052 V.

Table 4.6. Standard deviation of output voltage level at maximum cut-off frequency

Topology	**Load**	**F_{max}, MHz**	**V_{SET_HV}, V**	**V_{MEAN}, V**	**STD, V**
Half-bridge	50 Ω	35.0	200	177.64	1.623
	2 nF	12.8	25	17.58	0.052
Transformer gate drive	50 Ω	32.0	200	144.51	0.524
	2 nF	15.0	30	21.21	0.098
Push-pull	50 Ω	35.0	200	198.11	2.792
	2 nF	12.2	15	10.62	0.074

For each of the pulser topologies the signal propagation delay is measured (Table 4.7). An increase in rise time was seen when loaded with capacitive loads, which was due to increased rise time of the output signal. Rise time was measured 5 times and the mean value, and the standard deviation are shown in the table below. As expected from the nature of half-bridge topology shows the longest propagation delay due to use of opto-isolators. The CPLDs used in all topologies are identical, and the only other component that can deliver an extended propagation delay is the gate driver. When compared with transformer gate-drive topology, the additional delay from this circuit around 9 ns. Push-pull topology shows the lowest delay times out of all topologies and reaches 24.1 ns with 50 Ω load, while transformer gate topology only achieves 31.2 ns delay time at the same load. Standard deviation in all cases is withing tolerance, showing the consistency of the measured propagation delay values.

Table 4.7. Propagation delay of tested topologies

Topology	**Half-bridge**				**Transformer gate drive**				**Push-pull**			
Load	50 Ω	470 pF	1 nF	2 nF	50 Ω	470 pF	1 nF	2 nF	50 Ω	470 pF	1 nF	2 nF
Mean prop. delay, ns	40.5	45.8	50.3	55.3	31.2	36.2	40.2	46.0	24.1	30.3	35.5	43.1
STD, ns	0.09	0.16	0.19	0.25	0.19	0.09	0.28	0.05	0.07	0.25	0.09	0.08

Energy used from the high voltage power supply were measured for all three topologies (Fig. 4.31). It is expressed as the mean energy to form a single bipolar pulse. Energy per pulse was measured with 10 pulses of 1 MHz signal repeating every 1 ms, the mean current was measured using a digital multimeter and noted, Formula (3.1) was used in calculating energy value. Push-pull topology exhibits the highest energy per pulse values, while half-bridge and transformer gate drive topology show similar results. It must be noted that in brief the transformer gate drive topology experienced the least losses on the high voltage power source, notably around three times less than push-pull topology.

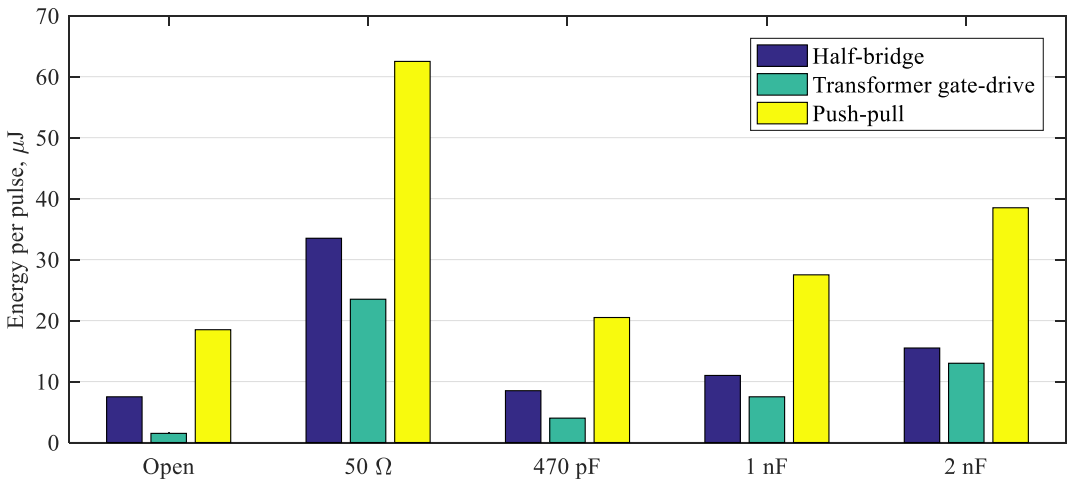

Fig. 4.31. Energy per pulse of topologies under test

To conclude the measurement results in a single graph a spider graph is used (Fig. 4.32). In brief, the better performance is indicated by the outermost edge of the graph, while centre represents less wanted values. In the diagram the best and the worst-case scenarios are taken into consideration. Maximum frequency for a pure resistive load is achieved by the half-bridge and push-pull topologies. With the capacitive load of 2 nF push-pull topology falls behind other competitors, and transformer gate drive topology achieves the highest output frequency of 15.0 MHz. When considering energy used per pulse, push-pull topology falls far behind rest of the topologies. In the case for 2 nF load, both transformer gate drive and half-bridge energy per pulse can be considered very similar. Half-bridge topology excels excellent rise time for the worst-case load. Transformer gate drive topology shows the slowest rise time for 2 nF load, despite achieving the highest frequency with this load. Push-pull topology shows fastest propagation delay for both best (50 Ω) and worst case (2 nF) scenarios, while propagation delay for the half-bridge topology is the longest. This can be attributed to the low voltage signal isolation ICs used to galvanically isolate gate driving control signals between the control CPLD and gate driver IC. With all the considerations mentioned above, the transformer

gate-drive topology is chosen for improvement and evaluation, using new generation gallium nitride transistors.

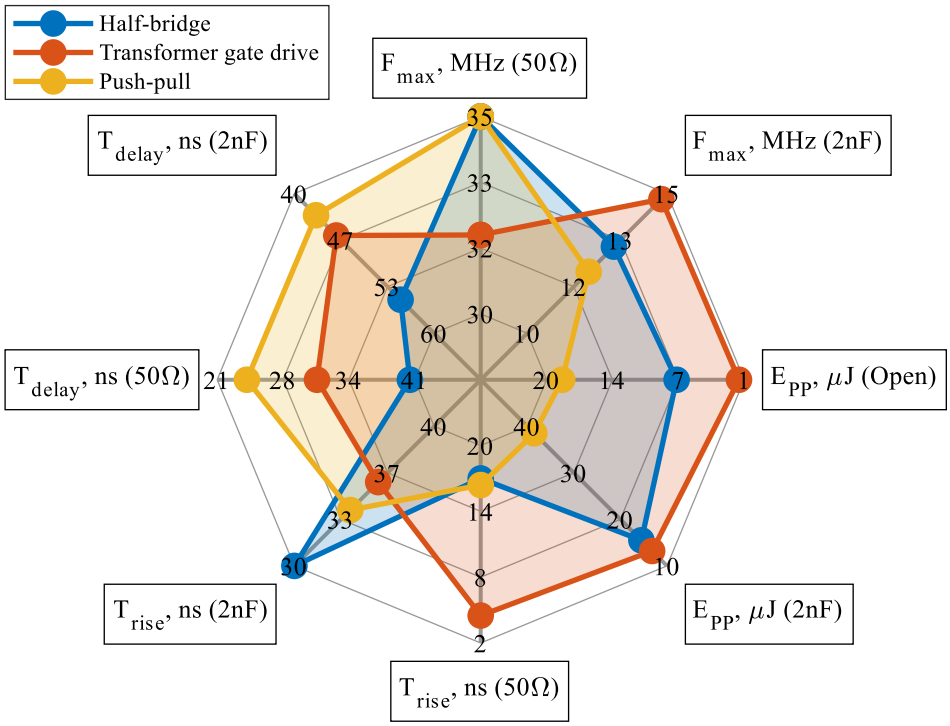

Fig. 4.32. Spider diagram of the main parameters of pulsers under test

5. On performance improvement by using new generation transistors

Gallium nitride transistors were chosen as the main mean to improve the current pulser design. As discussed in Chapter 2, SiC transistors are excellent for high voltage and high current applications, but lack the capabilities for high speed switching. The improvement possibilities for high voltage pulser, using gallium nitride transistors over silicon super-junction IPD60R2K0C6 MOSFET, will be tested using two different transistors (Table 5.1).

Table 5.1. Main parameters of GaN and Si transistors used in the experiment

Transistor	Technology	V_{max}	I	Q_G	C_{ISS} (50 V)	C_{OSS} (50 V)	C_{RSS}	R_G	R_{DS}
IPD60R2K0C6	Si SJ	650 V	6.0 A	6.7 nC	140 pF	40 pF	8.5 pF	12 Ω	1.8 Ω
TP65H300	eGaN	650 V	6.5 A	9.6 nC	760 pF	60 pF	2.0 pF	-	240 mΩ
GS-065-004	eGaN	650 V	4.0 A	2.2 nC	70 pF	20 pF	0.4 pF	1.4 Ω	450 mΩ

As a comparison between chosen transistors figure of merit can be calculated using Formula (2.6) by using output capacitance at 50 V and 200 V. Equivalently, results are FOM_{1A} and FOM_{1B} in (Table 5.2). By using Formula (2.7) alternative figure of merit is found – FOM_2. In both cases, lower number means lower losses, thus better switching performance.

Table 5.2. Figure of merit for selected transistors

Transistor	FOM_{1A}	FOM_{1B}	FOM_2
IPD60R2K0C6	$2.160 \cdot 10^{-11}$	$7.200 \cdot 10^{-11}$	$1.206 \cdot 10^{-08}$
TP65H300	$3.840 \cdot 10^{-12}$	$2.700 \cdot 10^{-11}$	$2.304 \cdot 10^{-09}$
GS-065-004	$3.150 \cdot 10^{-12}$	$4.800 \cdot 10^{-12}$	$3.600 \cdot 10^{-10}$

As seen from the table above, the TP65H300 transistor does have a higher output capacitance but due to much lower drain-source resistance it experiences lower losses. By inducing less energy into heat, the die remains cooler and experiences lesser drain-source resistance growth. The rise of the drain-source resistance can reduce the output current thus also reducing the speed of charging of the capacitive load. This leads to poorer performance with high frequencies, as a direct consequence of longer rise/fall times.

To test the use of gallium nitride transistors in transformer gate-drive topology pulser prototype printed circuit boards were made at the university laboratory (Fig. 5.1). As all tested transistors used different footprints, different versions of the output stage were made and attached to the logic board, which remained the same for all the tests of eGaN FETs.

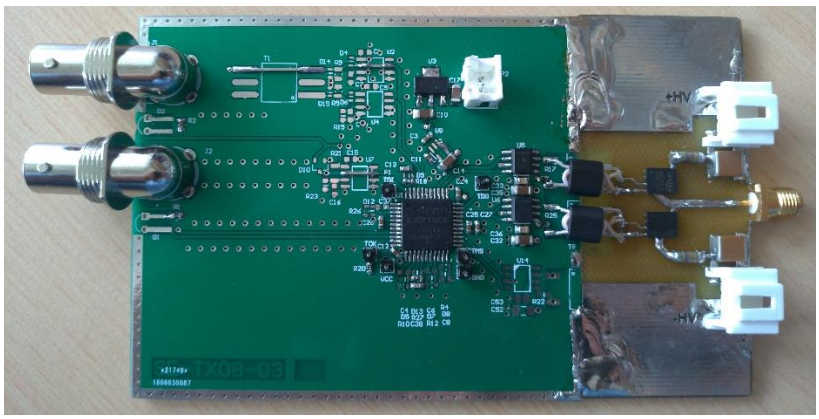

Fig. 5.1. Test PCB of the eGaN FET GS-065-004

All the transistors are tested using the same loads, used to test different topologies. The internal gate resistance of the TP65H300 transistor is not specified by the manufacturer. To keep the test in the same conditions, the external gate resistor is being kept the same: 4.7 Ω for the TP65H300 transistor. For the GS-065-004 transistor this resistance is increased to 8.2 Ω. This was a necessary action due to severe oscillations occurring on the output of the transistor (Fig. 5.2).

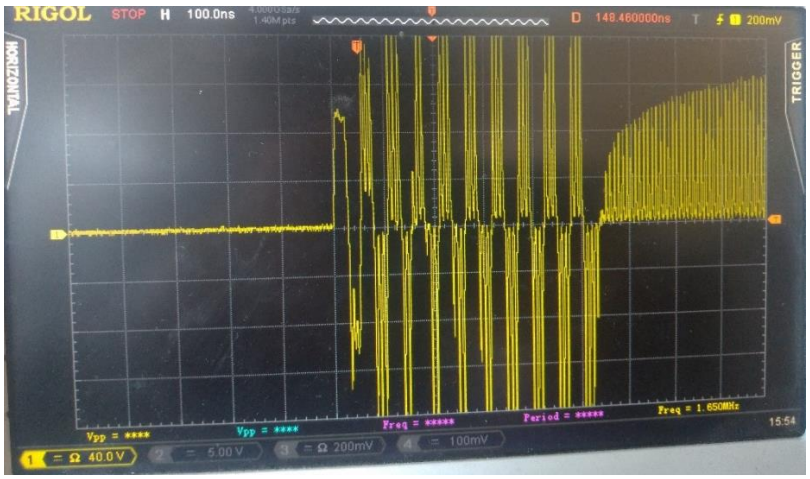

Fig. 5.2. Oscillations occurring on the output of the pulser (20 MHz, 100 V, 470 pF load)

5.1. Gallium nitride transistor GS-065-004

The results of the cut-off frequency are shown in (Fig. 5.3). The transformer gate topology enhanced with eGaN FET achieves over 50 MHz of output frequency with a 50 Ω load. For capacitive loads, the improvements in output capabilities can also be observed. With a 470 pF load, a frequency of 37.1 MHz is achieved at 5 V output stage voltage. With 300 V on the output stage, 30.7 MHz can be achieved. With 1 nF and 2 nF loads, maximum frequencies of 24.9 MHz and 15.5 MHz are reached at 5 V on the output stage. With increased voltage, the maximum frequency drops in value to 16.4 MHz for 1 nF load and 11.3 MHz for 2 nF load at 300 V on the output stage.

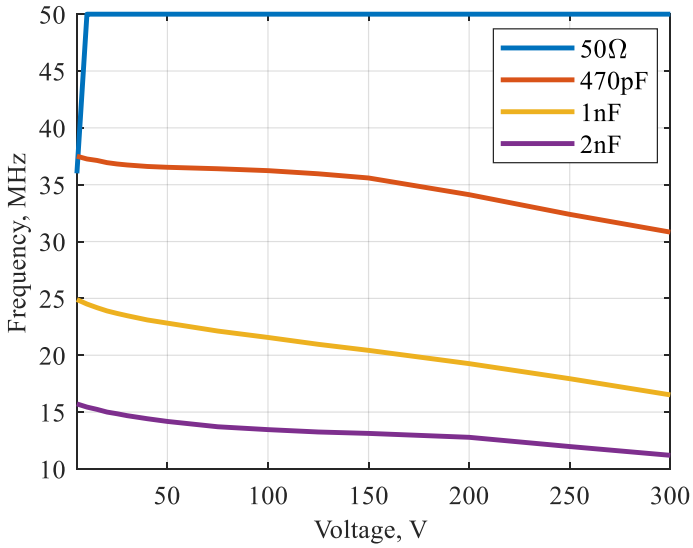

Fig. 5.3. Cut-off frequency of GS-065-004 eGaN FET based pulser found by SWC result

An output level map was made (Fig. 5.4). With a capacitive load of 470 pF the peak output is reached with a 20 MHz signal. This peak stretches from the 5 V to 300 V. With an increased capacitive load, a phenomena of very rapid amplitude decline is observed. In the case of 470 pF load the rapid amplitude decrease after a certain point might be possible. But as the upper frequency was limited to 38 MHz, that is impossible to state to be true. With 1 nF and 2 nF loads, a much steeper decline is observed at 100 V, as the output amplitude drops just under -6 dB boundary.

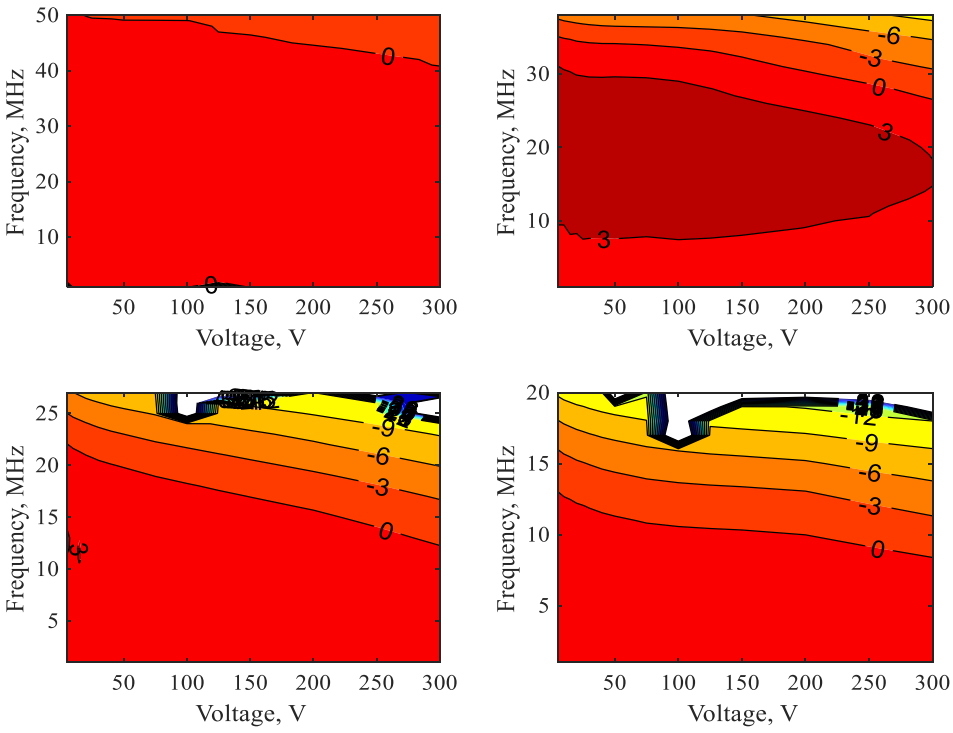

Fig. 5.4. Output of the pulser using GS-065-004 eGaN FET with 50 Ω load (top left), 470 pF load (top right), 1 nF load (bottom left) and 2 nF load (bottom right)

Rise time at signal of 1 MHz is measured (Fig. 5.5) and the possible maximum frequency is found (Fig. 5.6). When observing 470 pF and 50 Ω loads, a stability in rise time over increased voltage can be seen. For 1 nF and 2 nF loads and increase in rise time with an increase of the voltage is noticeable. From the calculated frequency the maximum frequency for 470 pF load is nearing 27 MHz to 29 MHz limit over the whole voltage range. With a 2 nF capacitive load, a stable frequency of around 10 MHz is found. The maximum frequency for 50 Ω resistive load, calculated from the rise time of 1 MHz signal, reaches 80 MHz and. This must be taken lightly as it is beyond the capabilities of the test equipment in use to find the real cut-off frequency for 50 Ω load.

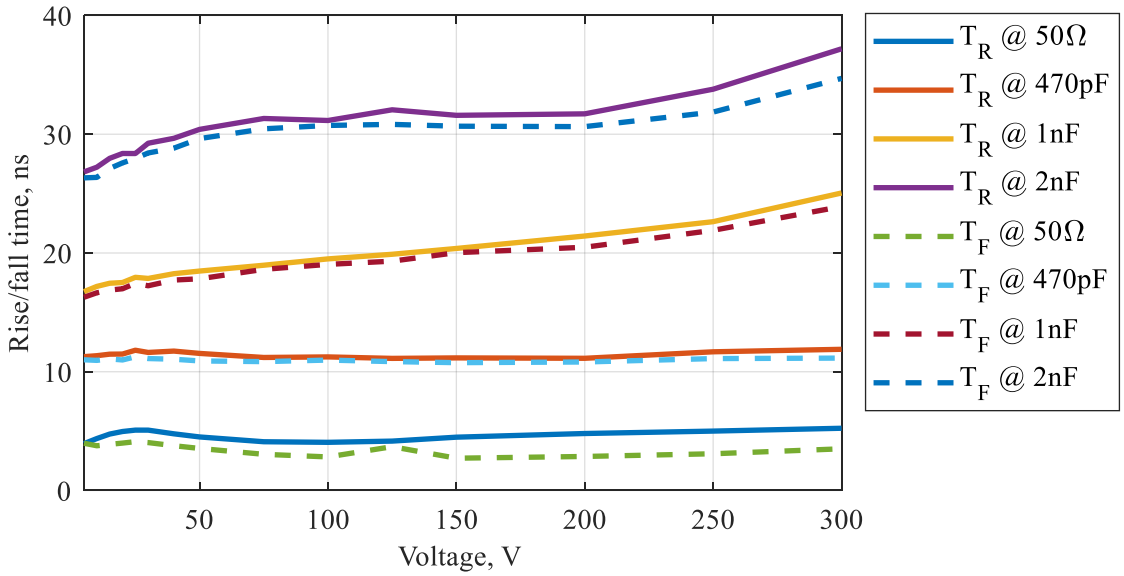

Fig. 5.5. Rise and fall times of GS-065-004 eGaN FET based pulser output

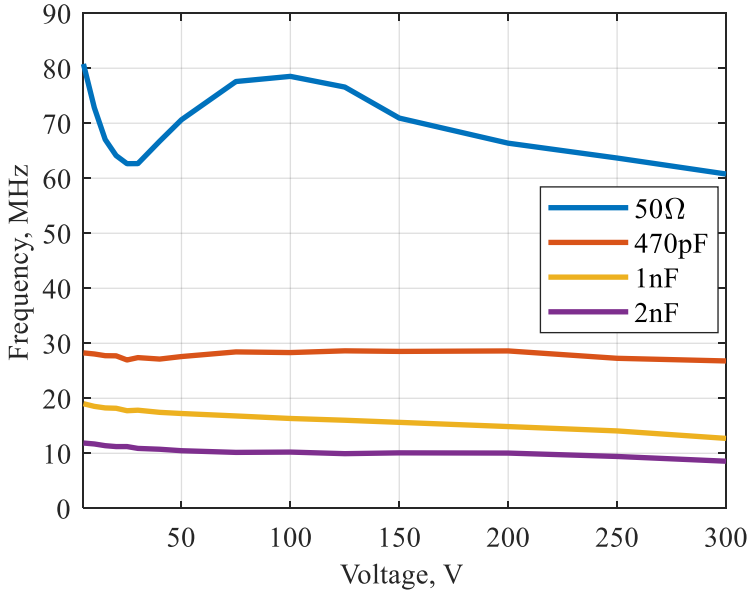

Fig. 5.6. Cut-off frequency of GS-065-004 based pulser derived from signal rise time at 1 MHz

When analysing time difference of set and measured pulse widths (Fig. 5.7), the 50 Ω excels excellent results, with traversing the 10 % limit only on several occasions at 200 V and 300 V and not reaching

15 %. In both cases a very stable output signal is observed. With 2 nF load the pulse width difference increases below 50 ns pulse width. And for 1 nF and 470 nF loads the limit is 25 ns and 14 ns, respectively.

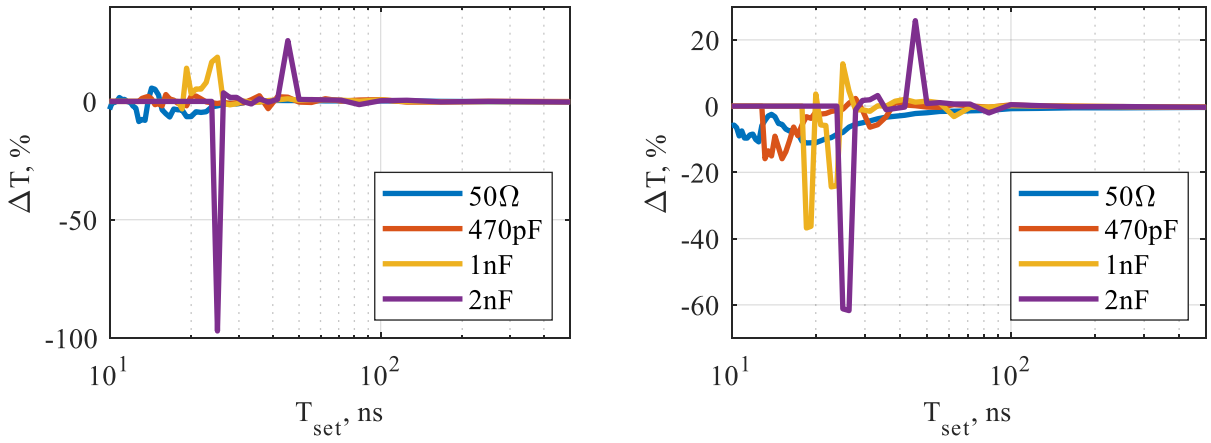

Fig. 5.7. Time difference vs set pulse width for GS-065-004 transistor based pulser at 50 V (left) and 200 V (right)

5.2. Gallium nitride transistor TP65H300

The results of the cut-off frequency are shown in (Fig. 5.8). The transformer gate topology enhanced with eGaN FET TP65H300 achieves 27.5 MHz of output frequency with a 50 Ω load. With a 470 pF load, a frequency of 24 MHz is achieved at 20 V output stage voltage. With 300 V on the output stage, 18 MHz can be achieved. With 1 nF and 2 nF loads, maximum frequencies of 20 MHz and 15 MHz are reached below 20 V on the output stage. This is due to a wrong assumption about the output of the pulser and signals above 20 MHz for 1 nF load and 15 MHz for 2 nF load were not tested. At 300 V on the output stage, the maximum frequency drops in value to 13.5 MHz for 1 nF load and 11 MHz for 2 nF load.

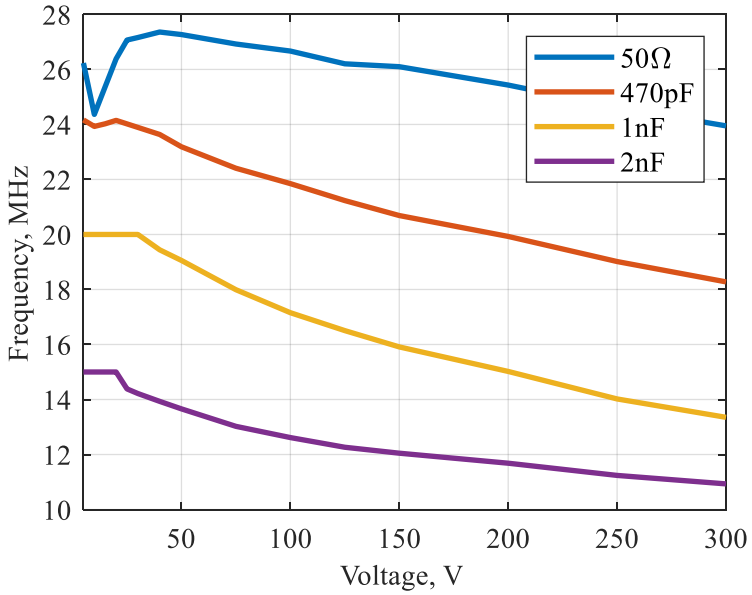

Fig. 5.8. Cut-off frequency of TP65H300 GaN FET based pulser found by SWC result

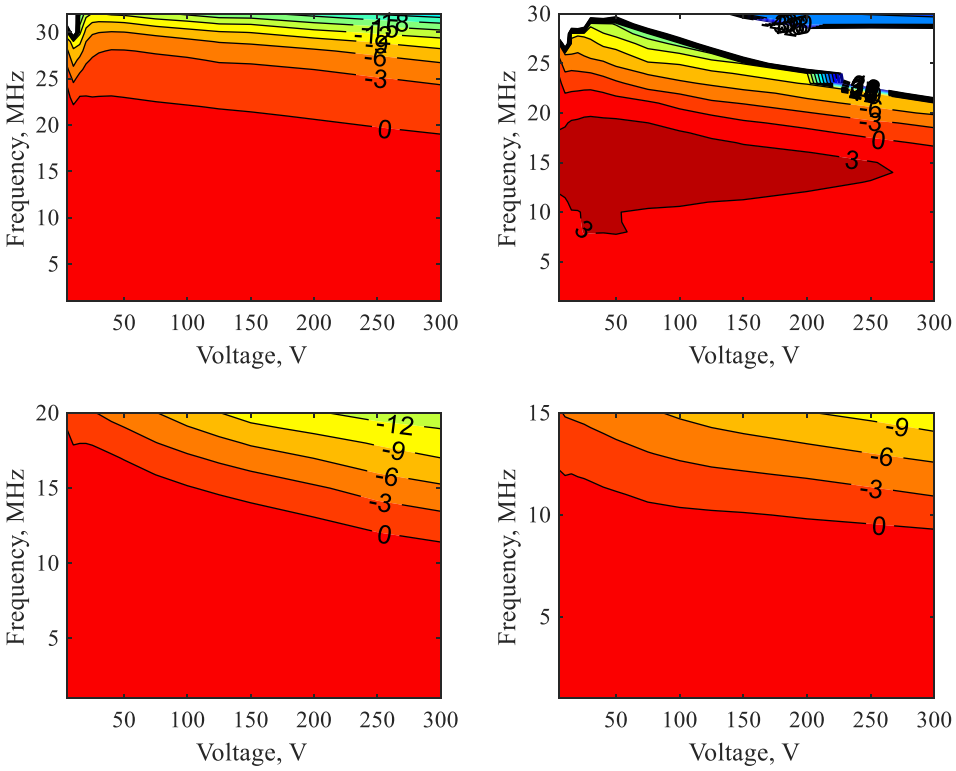

Fig. 5.9. Output of the pulser using TP65H300 eGaN FET with 50 Ω load (top left), 470 pF load (top right), 1 nF load (bottom left) and 2 nF load (bottom right)

From the output level map (Fig. 5.9), the output of the 50 Ω load is similar to the one seen in topology comparison. But in this case the cut-off frequency is lower at 27.6 MHz. When observing 470 pF load, a steep amplitude decrease is observed as was the case with the GS-065-004 transistors. And due to lower set frequency limit, the output level map shows clipped results. But in general, the 1 nF and 2 nF load output level maps show the important – greater than -3 dB area, which has the main area of interest.

Rise time at signal of 1 MHz is measured (Fig. 5.10) and the possible maximum frequency is found (Fig. 5.11). When observing 470 pF load, a stability in rise time over increased voltage can be seen. For 50 Ω, 1 nF and 2 nF loads and increase in rise time with an increase of the voltage is noticeable. From the calculated frequency the maximum frequency for 470 pF load is nearing 30 MHz limit over the 100 V – 200 V range. When loaded with 1 nF capacitor a peak frequency of 17 MHz is observed at 40 V. With a 2 nF capacitive load, a stable frequency of around 10 MHz is found.

The rise times for the TP65H300 eGaN FET are very similar to the rise times of GS-065-004 eGaN FET, with only difference being the 50 Ω load. For the 470 pF and 2 nF loads, both transistors achieve equal rise times of roughly 12 ns and 32 ns accordingly. The cut-off frequency derived from rise time for 50 Ω shows frequencies in excess of 50 MHz. Although the rise times of the capacitive loads closely match the rise times of the GS-065-004 transistor, the actual output performance differs. In almost all cases the performance of the TP65H300 transistor closely matches the performance of the IPD60R2K0C6 MOSFET used in topology comparison.

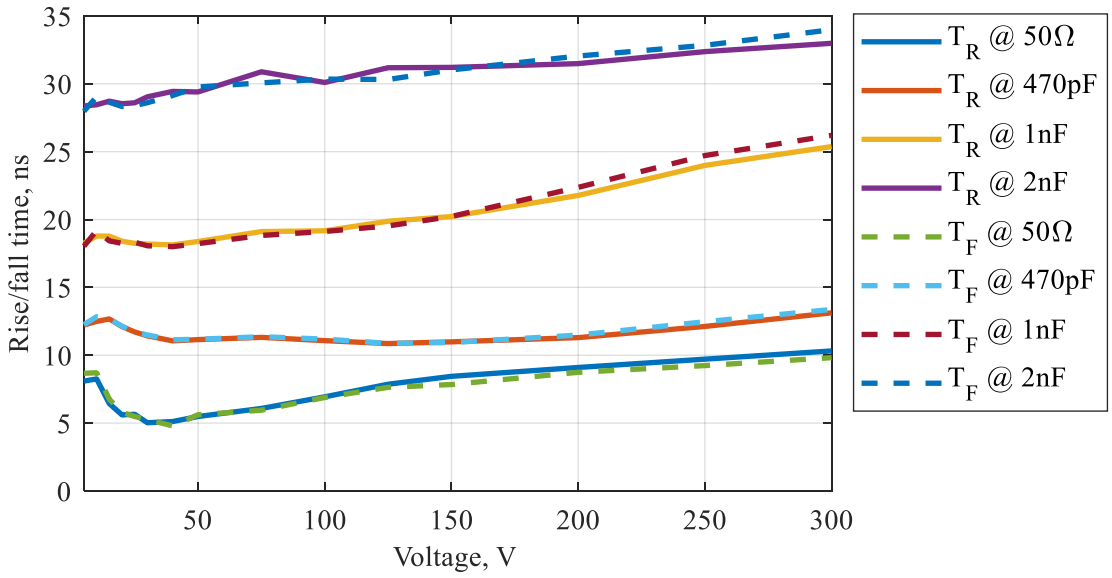

Fig. 5.10. Rise and fall times of TP65H300 eGaN FET based pulser

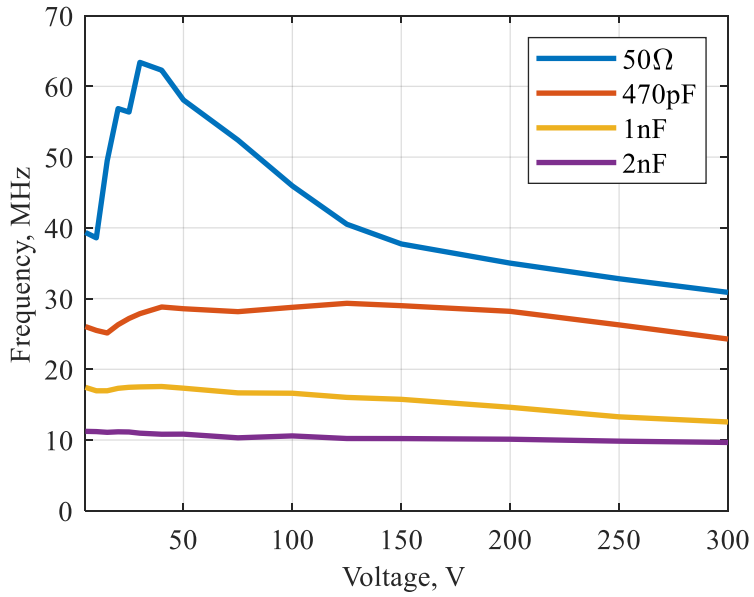

Fig. 5.11. Cut-off frequency of TP65H300 based pulser derived from signal rise time at 1 MHz

When analysing time difference of set and measured pulse widths (Fig. 5.12), the 50 Ω excels excellent results, with achieving stable output pulse width up to 23.8 MHz. When loaded with 470 pF capacitance, the maximum frequency is estimated at 16 MHz. And for 1 nF and 2 nF loads, the limit of 10 % difference in set and actual pulse width is at 11 MHz and 9 MHz equivalently.

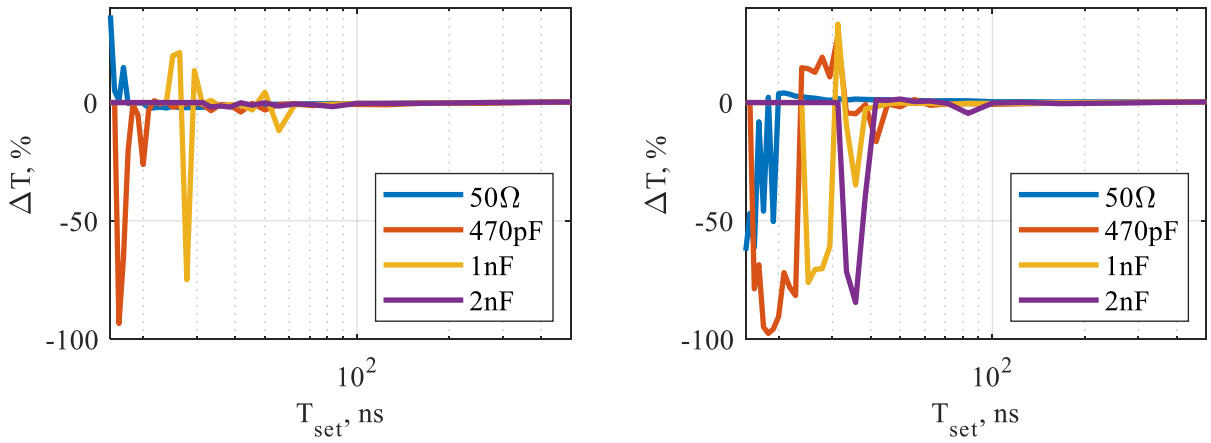

Fig. 5.12. Time difference vs set pulse width for TP65H300 transistor based pulser at 50 V (left) and 200 V (right)

5.3. Overview of the results

With all the results gathered and examined, final observations can be made. For both GaN transistor based pulsers, energy per pulse is measured and compared (Fig. 5.13) with the Si transistor used in the transformer gate-drive topology – IPD60R2K0C6. From results given in the (Fig. 5.13), it is observed that energy used to produce 1 MHz pulse trains can be interpreted as equal. The difference in the results can be assigned to reading the average current value from the ammeter (RIGOL DM3058E; sampling rate – 120 Hz). The energy per pulse values, measured for eGaN FET based transformer gate drive topology, do closely resemble the values observed with Si transistor based pulser. Thus, indicating the energy use assessment of the pulser topologies is valid and produces repeatable results. For eGaN FETs, the energy per pulse value is lower when compared with Si based pulser, although the statistical significance was not determined in this work.

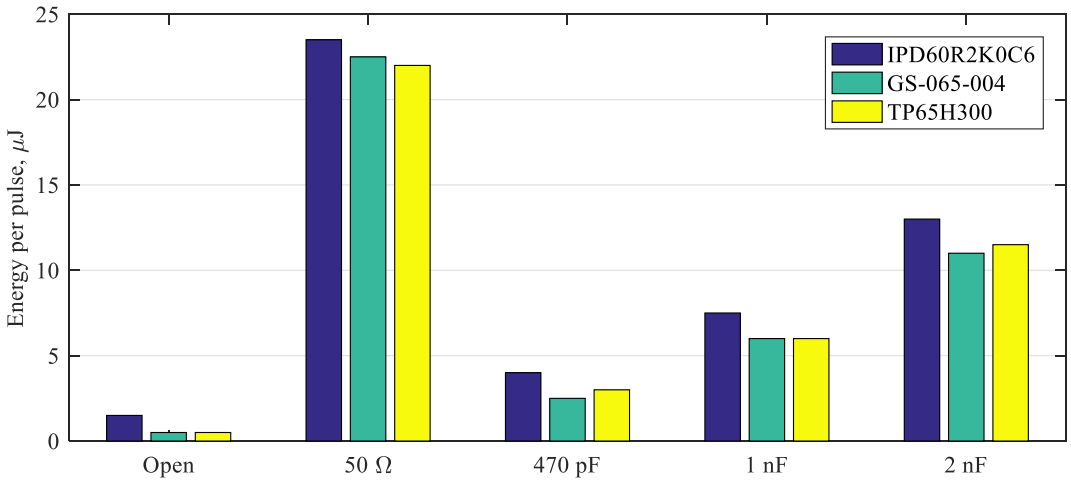

Fig. 5.13. Energy per pulse of eGaN FETs under test and IPD60R2K0C6 MOSFET

As was the case in topology comparison, the key points – maximum achievable frequency at different loads, rise time and propagation delay are measured with a sample size of 10 to make sure the

deviations of the measurements are within tolerable amount. Measured mean propagation delay times are given in (Table 5.3), standard deviation for the output level at cut-off frequency is given in (Table 5.4). When comparing propagation delay, an improvement over older pulser technology can be seen. A propagation delay difference of 3.3 ns over the whole load range for GS-065-004 based pulser is observed. For the TP65H300 eGaN FET based pulser a propagation time difference of 4.1 ns is seen. This clearly is a much lower delay variation when compared to the transformer gate-drive topology pulser which show a difference of 14.8 ns with an increasing load capacitance.

Table 5.3. Propagation delay of eGaN FET based pulser

Main transistor	**GS-065-004**				**TP65H300**			
Load	50 Ω	470 pF	1 nF	2 nF	50 Ω	470 pF	1 nF	2 nF
Mean prop. delay, ns	21.01	22.85	23.07	23.31	20.57	22.97	23.91	24.70
STD, ns	0.018	0.019	0.027	0.023	0.017	0.014	0.025	0.039

When comparing the output level deviation at the key points for 50 Ω and 2 nF loads, satisfying results are observed. The GS-065-004 transistor based pulser delivered 50 MHz signal at 89.56 V with the set value being 100 V. When comparing both transistors with 2 nF load, the peak frequencies were observed at low voltages – 5 V and 15 V. In both cases the standard deviation is 0.018 V and 0.038 V for the GS-065-004 and TP65H300 transistors, respectively.

Table 5.4. Standard deviation of the output voltage at cut-off frequency

Main transistor	**Load**	**F_{max}, MHz**	**V_{HV}, V**	**V_{MEAN}, V**	**STD, V**
GS-065-004	50 Ω	50.0	100	89.56	1.151
	2 nF	15.7	5	3.55	0.018
TP65H300	50 Ω	27.6	40	28.28	0.046
	2 nF	15.0	15	11.08	0.038

The reduction in propagation delay partly can be contributed to the use of a faster CPLD. The newer CPLD has a propagation delay time of 2.5 ns against 10 ns for the CPLD used in topology comparison. Without the exception of decreased propagation delay, no other significant improvement can be contributed to the faster CPLD, as declared rise times of the output signals are identical for both CPLDs.

To showcase the results in comparing Si and GaN transistors a spider diagram is used (Fig. 5.14). It is important to note the axis limits of the graph, many of the axis have been zoomed in to show a clearer difference in the values of the parameters. When driving a resistive load, the GS-065-004 transistor show the most excellent results and successfully reaching 50 MHz signal. With a 2 nF load the IPD60R2K0C6 and TP65H300 show almost identical results of 15.0 MHz each, while GS-065-004 shows slightly improved performance of 15.7 MHz. As discussed previously, energy per pulse improvements can be noticed but they are very slim. Rise time with 50 Ω load shows very close results varying only from 4 ns to 5 ns for GS-065-004 and TP65H300 transistors with IPD65R2K0C6 having a 4.5 ns rise time. When it comes to the rise time with a capacitive load of 2 nF, the GaN transistors display rise times of 27 ns and 28 ns, while the Si MOSFET has a rise time of 36 ns. Propagation delay for the GaN transistor based pulser is around 9 ns faster than a Si MOSFET based pulser.

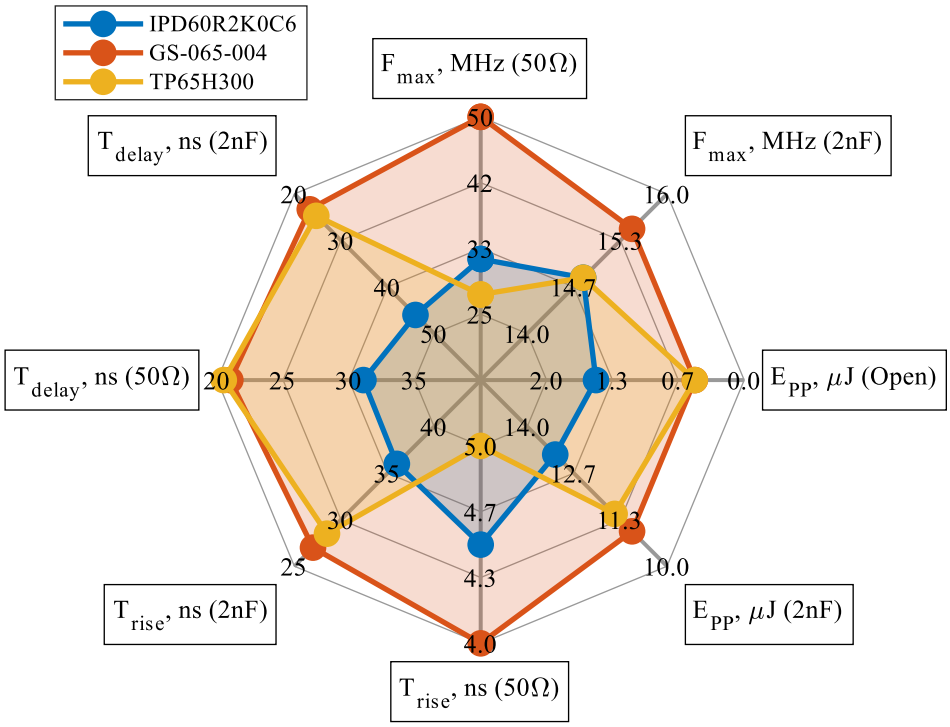

Fig. 5.14. Spider diagram of the main parameters of transistors used in transformer gate drive topology

Conclusions

1. Different topology pulsers were investigated and their ability to generate high voltage, high frequency pulses were compared using different parameters and methods. GaN transistors were implemented in the transformer gate-drive topology and performance improvements were noticed.
2. The paper overview of the topologies used in generating high voltage pulses showed different strong and weak points. Pulsers based on AB, B and D class power amplifiers did not meet the requirements of being able to generate the wanted output signal of high frequency, wide band output signal. This also led to some consideration about the physical size of the pulsers and the energy efficiency as being implemented into a battery powered device is one of the possible applications. The three main contenders were chosen: half-bridge, transformer gate-drive and push-pull topologies.
3. Analysis shows that with improvements in the semiconductor materials, transistors made of silicon carbide and gallium nitride are becoming more common in the market. With improved breakdown voltage, higher electron mobility and lower conductive channel resistance and lower parasitic capacitances and inductances, the benefits of new generation transistors are needed to achieve higher output frequencies and energy efficiency of high voltage pulsers.
4. The pulser topologies were tested for maximum achievable frequency. From the maximum frequency, achievable at different loads, only slight differences were observed, although the transformer gate-drive topology shows altogether higher output frequency over all tested capacitive loads (29.1 MHz for 470 pF load and 15.0 MHz with 2 nF load). The half-bridge and push-pull topologies show 12.8 MHz and 12.2 MHz respectively with 2 nF load.
5. When considering other parameters, it was observed that the transformer gate-drive topology shows better rise time with a resistive load (4.5 ns) and the lowest energy per pulse with 2 nF (13 μJ). Half-bridge topology experienced the fastest rise time with the 2 nF capacitive load, reaching a minimum rise time of 30 ns. Propagation delay is the lowest in the push-pull topology (23.1 ns with 50 Ω load and 43.1 ns with 2 nF load), while the half-bridge topology has the longest propagation delay (40.5 ns with 50 Ω load and 55.3 ns with 2 nF load).
6. Found and calculated parameters were considered to compare the maximum output performance of the pulsers. The SWC was used as a trusted reference metric for maximum achievable frequency by the pulser. Rise time measured at 1 MHz signal can show the possible output frequency performance, and results found by it do correlate with SWC results. When performing signal correlation with an ideal square wave, good results were observed for half-bridge and transformer gate-drive topology, and the results gotten from it closely resemble the SWC results. For the push-pull topology the method of correlation with a square wave is not viable due to output signal being greatly different from an expected output signal at frequencies higher than couple of megahertz.
7. Transformer gate-drive topology was chosen to be used as the benchmark to test two GaN FETs and compare the performance with IPD60R2K0C6 MOSFET. GS-065-004 shows great performance improvement over silicon MOSFET, reaching 37.1 MHz with 470 pF load and 15.5 MHz with 2 nF load. The TP65H300 eGaN FET shows very similar results as the silicon MOSFET and in some cases even a lower frequency was achieved with a resistive load. But the eGaN FET TP65H300 shows excellent propagation delay time of 20.57 ns and a rise time of 5 ns with the resistive load.

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