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Disturbance Rejection and Control Design of MVDC Converter with Evaluation of Power Loss and Efficiency Comparison of SiC and Si Based Power Devices

Faisal Mehmood Shah [1], Sarmad Maqsood [2] and Robertas Damaševičius [2,*] and Tomas Blažauskas [2]

[1] School of Electrical & Electronic Engineering, North China Electric Power University, Beijing 102206, China; shahfaisal94@gmail.com

[2] Department of Software Engineering, Kaunas University of Technology, 51368 Kaunas, Lithuania; sarmad.maqsood@ktu.edu (S.M.); tomas.blazauskas@ktu.lt (T.B.)

* Correspondence: robertas.damasevicius@ktu.lt

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Abstract: With direct current (DC) power generation from renewable sources, as well as the current relocation of loads from alternating current (AC) to DC, medium-voltage DC (MVDC) should fill gaps in the areas of distribution and transmission, thereby improving energy efficiency. The MVDC system is a platform that interconnects electric power generation renewables (solar, wind) with loads such as data centers, industrial facilities and electric vehicle (EV) charging stations (also using MVDC technology). DC–DC power converters are part of the rising technology for interconnecting future DC grids, providing good controllability, reliability and bi-directional power flow. The contribution of this work is a novel and efficient multi-port DC–DC converter topology having interconnections between two converters, three-level neutral point clamping (NPC) on the high-voltage (HV) side and two converters on the low-voltage (LV) side, providing two nominal low voltages of 400 V (constant) and 500 V (variable), respectively. The design of this new and effective control strategy on the LV side has taken into condition load disturbances, fluctuations and voltage dips. A double-closed-loop control topology is suggested, where an outside voltage control loop (in which the capacitance energies are analyzed as variable, and the inside current loop is decoupled without the precise value of boost inductance) is used. The simulation results show the effectiveness of the proposed control system. In the second part of this study, wide-bandgap SiC and Si devices are compared by using comprehensive mathematical modeling and LT-spice software. Improving power loss efficiency and overall cost comparisons are also discussed.

Keywords: bi-directional; medium-voltage DC–DC converter; silicon-carbide; neutral point clamping; double-closed-loop

1. Introduction

Direct current (DC) network systems are being analyzed and explored for use in future transmission and distribution technology due to advancements and maturity in the power electronic devices. Medium-voltage DC (MVDC) systems fill the gap in transmission and distribution areas, improving efficiency and energy delivery. In the future, MVDC grids would be the most flexible technique to collect renewable energy (e.g., solar, wind farms) and within industrial and urban area distribution networks. DC–DC high-power converters play a major role in the interconnection to MVDC grids, which must be capable to deal with unidirectional or bi-directional power flows.

Compared to the medium-voltage alternating current (MVAC) system, the MVDC system shown in Figure 1 reduces cable weight, avoiding voltage dip problems at many points and easily parallels generators [1–8]. Moreover, most equipment in use employs DC; therefore, conversion stage losses will be reduced, and as a result the economy and efficiency could be improved [9]. However, MVDC acts as a foundation for developing a smart transportation system, which includes all electric trains, vehicles, planes and ships. Industrially, the first MVDC link between the UK and North Wales has recently been announced. The DC ANGLE project connects to the island of Anglesey by the Llanfair PG substation and to the North Wales mainland with Bangor operating at 27 kV DC along a 30.5 MW rating [10,11]. Due the recent development of new silicon carbide (SiC)-based semiconductor power devices, their use in markets is increasing due to their effectiveness and useful properties, such as significantly reducing conduction losses and switching losses in power converters, as well as improving converter efficiency. Thus, in many applications they would considered as an alternative to Si [12–18]. Currently, power semiconductor devices in the market (e.g., (SiC) silicon carbide MOSFET, Insulated Gate Bipolar Transistors (IGBTs)) are still expensive as compared to traditional Si (silicon). Consequently, this increases the cost of system, especially for higher-power converters that require a large number of power semiconductor devices. However, reducing the number of wide-bandgap (WBG) devices used in power converters will go a long way in the present industry in reducing costs [19].

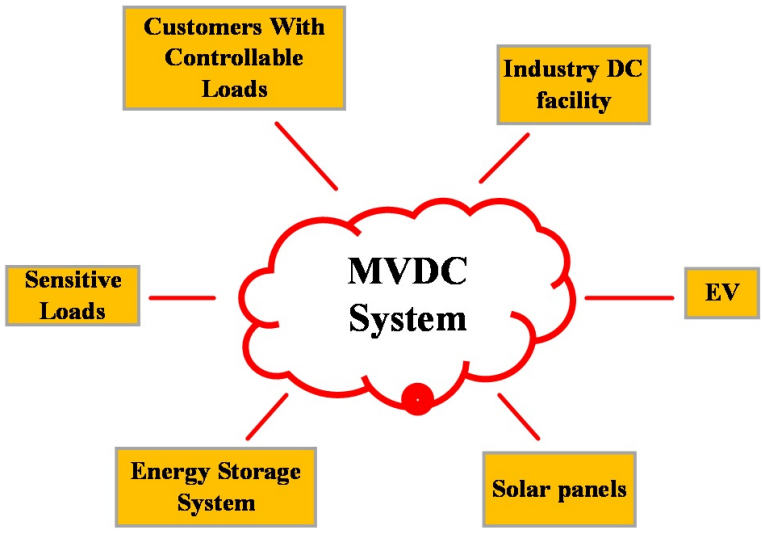


Figure 1. Applications of the medium-voltage DC (MVDC) system.

In MVDC systems, the DC–DC converter is a key element, which acts as a transformer in current AC systems. The DC-based system performance depends on the DC converters because converters are responsible for changing voltage levels between the DC-based systems and delivering power. Therefore, the DC–DC converter has good reliability and performance, as needed for DC grids [10,20]. The DC–DC converter, which acts as the DC transformer, is one of the major key components in modern DC power grids and is connected to DC lines with variable voltage levels to make a DC network [21,22]. The MVDC DC–DC converter has drawn much attention in recent years; however, there are a number of major issues including protection and fault isolation, DC voltage regulation, output voltage control, voltage dip control, maintaining reliability and interconnecting different power lines [22–26]. All these DC–DC converters would have regulation capabilities, which provides balanced and stable voltage for back-end converters, improving system reliability and over-current control ability. In the MVDC power converters, Modular Multilevel Converter (MMC), flying capacitor, cascaded neutral point clamping (NPC) or active NPC (ANPC) topologies are usually used [27,28]. With an auto-transformer controlling two line-commutated current-sourced converters (LCCs), issues such as high-voltage DC (HVDC) interconnections, unreliability and power flow control are presented in [29]. Interactions between the

boost converter and disturbance rejection have been shown [30]. Bi-directional DC–DC high-efficiency interconnections in MVDC and HVDC converters have been discussed in combination with two-level MMCs [31–33]. Modeling of MVDC multidrive systems for power quality analysis and harmonic injection is discussed in [34]. Robust voltage control and parametric uncertainties considering DC–DC converters are shown in [35]. A practical DC fault ride-through method for MMC-based MVDC distribution systems is proposed in [36]. For future distribution networks, a new, fast-acting backup protection strategy for embedded MVDC links is suggested in [37]. Modeling of the power SiC MOSFET module and predicting electromagnetic interference (EMI) of MVDC railway electrification system are shown in [38]. A wide-bandgap heterogeneous power device for high-frequency applications was discussed in [39]. Fault-tolerant operations for different modes of MVDC are suggested in [32,40]. In [41], a three-phase triple-active bridge converter interconnected with the MVDC grid along two nominal voltages is described. However, comparisons of disturbance rejection, uncertainty and power losses for MVDC-based converters are not addressed in these works.

In [14], the control variable is set as the square of the DC-bus voltage, and DC-bus voltage is set as the control variable compared to the conventional method. In the present topology, the outside voltage control loop (in which the capacitance energies are analyzed as variable) method is suggested because it can minimize stress to the capacitance voltage and reduce capacitance voltage deviations. The current topology is for industrial applications that work with step-down voltages of DC voltage 10 kV to 400 V and 500 V. The proposed study is composed of two parts. In the first part, the performance and control scheme is articulated for multiport DC–DC, an interconnections between the two converters are presented. A three-level neutral point clamping (NPC) is used on the high-voltage (HV) side, and a two-level phase is used on the low-voltage (LV) side along a rectifier circuit using two high-frequency transformers (HFT), including two nominal voltages as shown in the block diagram in Figure 2. The HV side provides a nominal voltage of 10 kV, while the LV side provides a nominal voltage of 400 V DC and 500 V DC, respectively (system overview is shown in Table 1). On the LV side, in designing the new and effective control strategy, the conditions of load disturbance voltage fluctuations and non-serious voltage dips are taken into consideration. In this study the double-closed-loop control topology is used inside the current loop and outside the voltage loop control; the outer voltage loop control comprises two parts: the inner current loop is decoupled without an exact boost inductance value, and the voltage control loop is proposed in which the capacitance energy is analyzed as a variable. Provided a constant 400 V and allowing 2.3% variation during parallel load changing (according to the IEEE standard, 5% variation is acceptable [42]), the simulation results have shown that the proposed control topology is effective. The focus of this study is mainly on the LV side.

In the second part of the paper, SiC and Si semiconductor power devices are compared, in which the conduction loss and switching loss, wide range of switching frequencies, cost comparisons and overall performance are evaluated. An accurate mathematical model was developed to represent the DC–DC converter in which efficiency is measured by using the equations presented in Appendix A under 75% and full-resistive load conditions. Simulations were carried out in LTSpice software. Although SiC power devices have multiple benefits in several applications, this article is focused on enhancing the efficiency of DC–DC bidirectional converters.

This study is organized as follows: in Section 2, the proposed control topology configuration on the LV side is presented. In Section 3, the simulation results of the proposed converter are discussed. In Section 4, the comparisons of power semiconductor devices and loss calculations in different load conditions are presented. Finally, in Section 5 the efficiency and cost comparisons are discussed in detail.

Table 1. Converter parameter of the simulation.

Specifications	Values
Power Electronic Devices	IGBT/Diode
Port 1 nominal Input voltage	20 kV
Port 2 nominal output voltage	500 V
Maximum Power	15 kW
Port 3 nominal output voltage	400 V
Maximum Power	15 kW
Switching frequency $f(sw)$	20 kHz
Converter frequency	50 kHz
Sampling Frequency of the controller	20 kHz
Maximum Voltage Deviation	$\pm$10%
Filter capacitance (C)	30 µF
Filter Inductance (L)	0.8 mH
Kp_1 Light-load	0.15
Ki_1 Light-load	0.004
Kp_2 Light-load	0.06
Ki_2 Light-load	0.002
Kp_1 Heavy-load	0.8
Ki_1 Heavy-load	0.016
Kp_2 Heavy-load	0.2
Ki_2 Heavy-load	0.006
Cd_1, Cd_2 on LV side	4000 µ$F \times 2$
C_1, C_2 on HV side	$13 \times 10^{-3} F \times 2$
Modulation Index	0.8
Load Resistance	100 Ω

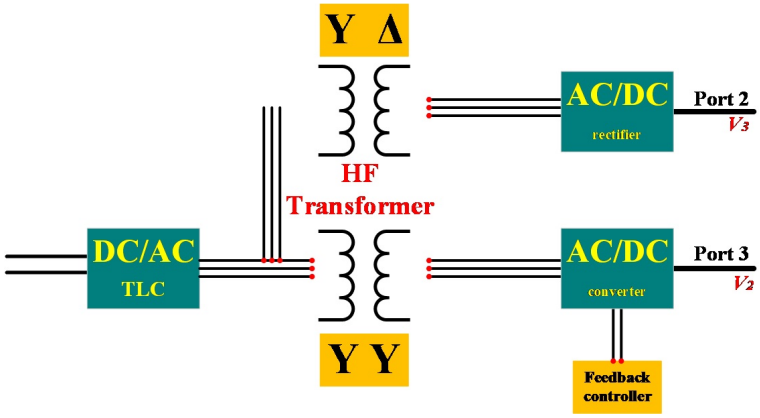


Figure 2. Block diagram of the proposed DC/DC converter.

2. System Modeling and Control of DC–DC Three-Level MVDC Converter

Usually, in low-power and LV configurations, the two-level inverter topology is more attractive, but in high-power and HV drive applications, the three-level NPC topology is better because it generates very low harmonic distortion sinusoidal voltage waveforms by using the space vector pulse width modulation (SVPWM) switching technique. In this study, on the HV side the three-level NPC topology has been simulated using the SVPWM technique. The control scheme on the HV side inverter is shown in Figure 3 by using MATLAB/Simulink. In this research the main focus is only on the LV side.

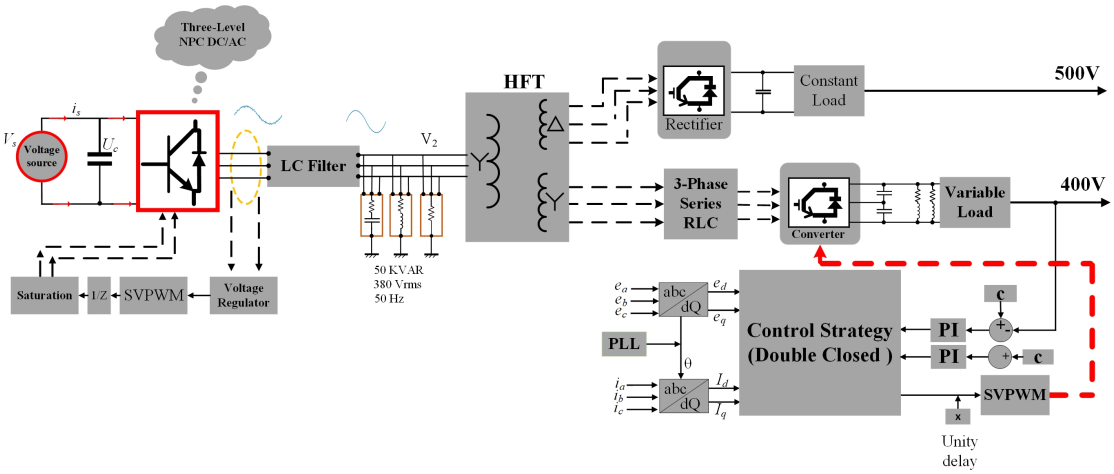


Figure 3. Proposed DC–DC MVDC converter.

3. Mathematical Model on the LV Side

Figure 4 [43] shows the power circuit of the three-phase voltage source rectifier topology. When designing this mathematical model we assumed a balanced three-phase system.

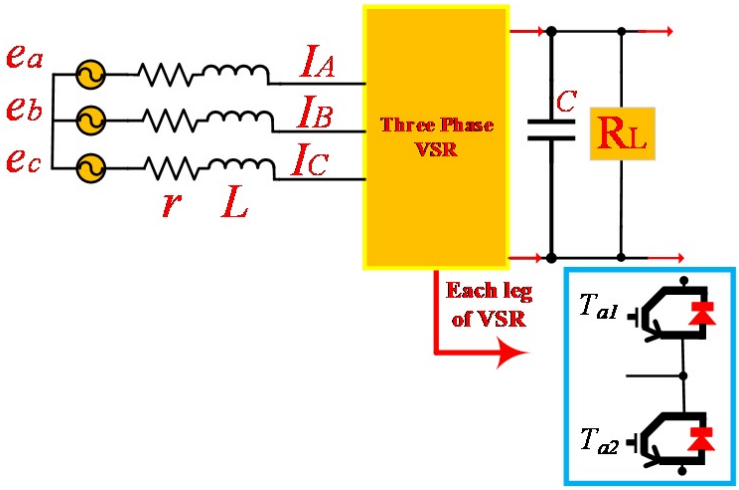


Figure 4. Three-phase voltage sensitive relay (VSR) circuit.

In the above figure, e_a, e_b and e_c are the source voltages; i_A, i_B and i_C are the line current; v_a, v_b and v_c are the input rectifier voltage; v_dc is DC output voltage; r is the resistance of the filter reactor; L is inductance of the filter reactor; R_L is load resistance; i_L is load current; VT_1 - VT_2 are IGBTs; s_j (j = 1-6) are switching functions,

The definition of switching function is

$$s_j \begin{cases} 1, s_j opened \\ 0, s_j closed \end{cases} \quad (1)$$

The three-phase model of the voltage-sourced Pulse Width Modulated (PWM) rectifier can be expressed in the stationary a-b-c frame as (1), when the three-phase AC sources are balanced and the resistance of the power circuit is ignored.

$$\begin{cases} L\frac{di_A}{dt} + ri_A = e_a - (v_a + U_{NO}) \\ L\frac{di_B}{dt} + ri_B = e_b - (v_b + U_{NO}) \\ L\frac{di_C}{dt} + ri_C = e_c - (v_c + U_{NO}) \\ C\frac{dv_dc}{dt} + i_A S_a + i_B S_b + i_C S_c - i_L \end{cases} \quad (2)$$

The symmetry of the three-phase current and voltage is

$$\begin{cases} v_j = v_{dc} * s_j, (j = a, b, c) \\ U_{NO} = -\frac{U_{dc}}{3}(s_a, s_b, s_c) \end{cases} \quad (3)$$

Performing the park transformation, the mathematical model in the synchronous $d-q$ rotating frame can be expressed as

$$\begin{cases} L\frac{di_d}{dt} + ri_d = e_d - v_d + \omega L i_q \\ L\frac{di_q}{dt} + ri_q = e_q - v_q + \omega L i_d \\ C\frac{dv_{dc}}{dt} = 1.5(i_d s_d + i_q s_q) - i_L \end{cases} \quad (4)$$

where v_d, v_q and s_d, s_q are input voltages and switching function of the rectifier in synchronous rotating $d-q$ coordinates, respectively.

3.1. LV Side Control Design and Mathematical Model

At present, advanced modern control theory is growing rapidly, which has led to new ideas and thinking to solve complex problems. However, many of the control strategies are more difficult to implement in the industrial applications. Relatively, in various control systems the conventional proportional–integral (PI) controller is widely used due to its robustness and briefness. Based on internal modern theory, Figure 5 shows the diagram of the controller. For sufficient and essential conditions for zero-state error, the closed loop contains $J_R(s)$ as the input generation model. Therefore, the open loop transfer function is $J_R(s) = F(s)\ C(s)$ and also must have the input generation model.

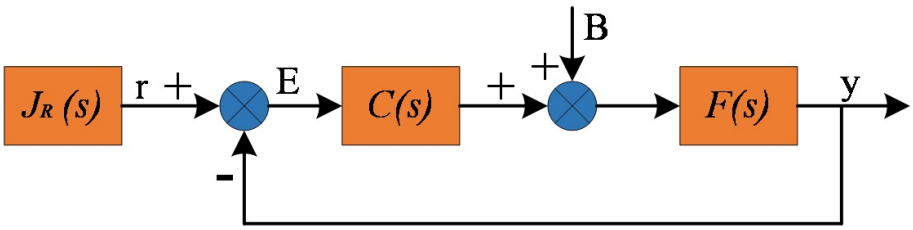


Figure 5. Internal model theory based controller.

Based on the internal model theory perspective, the zero steady-state error can be secured using the conventional PI controller , while the integration part contains s domain in the $1/s$ step signal. Therefore, to achieve the steady-state error the controller must contain a $\omega^2/(s^2 + \omega^2)$ part when the input signal is a sinusoidal $r(t)$, for example $Asin(\omega t)$, where the resonant controller is compulsory.

3.2. Design of Inner Current Loop

Figure 6 [44] shows the model of the three-phase voltage sourced rectifier $d-q$ frame.

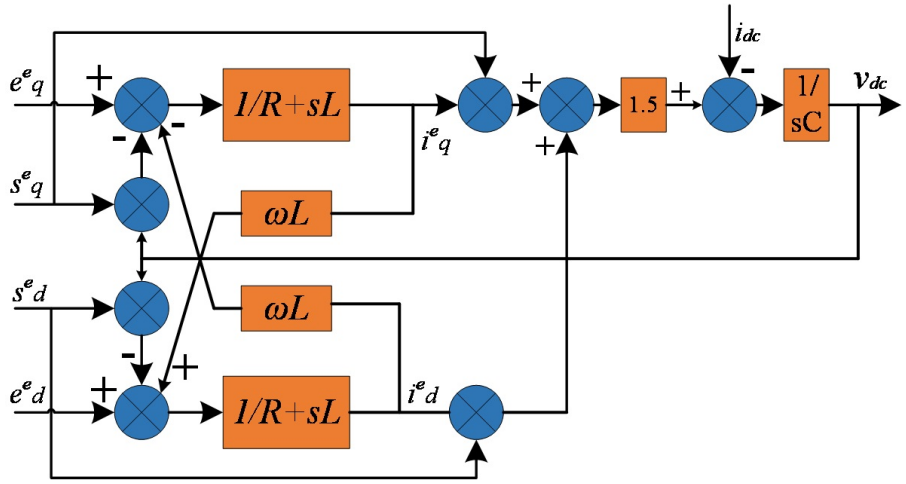


Figure 6. $d-q$ model of the three-phase voltage source rectifier.

Based on the synchronous $d-q$ rotating frame, the three-phase voltage-sourced rectifier and conventional control PI theory, the internal current loop is designed as follows:

$$\begin{cases} v_{dref} - e_d = -\left(K_{dP} + \frac{K_{di}}{s}\right)(i_{dref} - i_d) + \omega L i_q \\ v_{qref} - e_q = -\left(K_{qP} + \frac{K_{di}}{s}\right)(i_{dref} - i_d) + \omega L i_d \end{cases} \tag{5}$$

Figure 7 shows the obtained synchronous $d-q$ rotating frame and decoupling control diagram of the internal current loop. By using a conventional PI controller, the zero steady-state error can be secured because in the synchronous $d-q$ rotating frame the reference current is the constant DC signal.

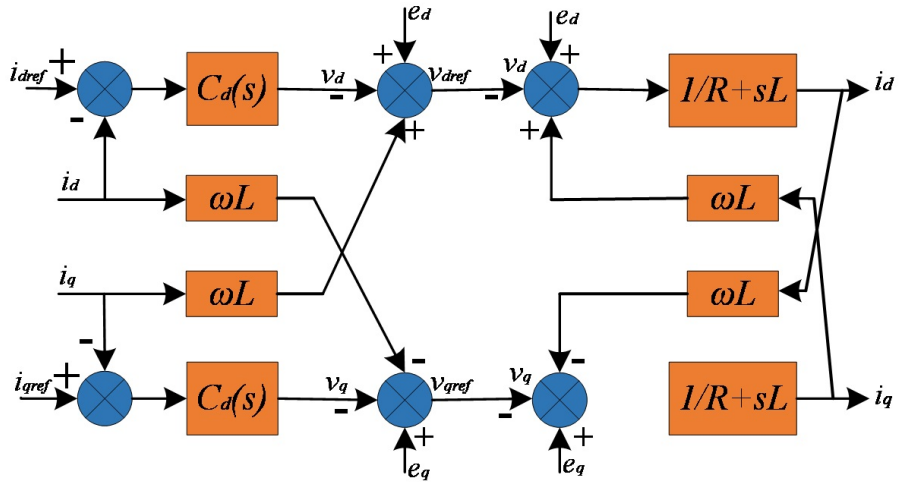


Figure 7. Decoupling control in the synchronous $d-q$ rotating frame.

where

$$\begin{cases} c_d(s) = \frac{K_{di}}{s} + K_{dP} \\ c_q(s) = \frac{K_{qi}}{s} + K_{qP} \end{cases} \tag{6}$$

Therefore, to completely decouple the $d-q$ axis, the exact value of inductance L is essential. In some extreme conditions the value of inductance L will be changed; thus, part of the decoupling is

often ignored. Hence, the enhanced coupling on the $d-q$ axis will lead to bad performance when the frequency increases.

With the model of the a-b-c three-phase rectifier, a two-phase $\alpha\beta$ reference frame model is obtained.

$$\begin{cases} L\frac{di_\alpha}{dt} = e_\alpha - v_\alpha - ri_\alpha \\ L\frac{di_\beta}{dt} = e_\beta - v_\beta - ri_\beta \end{cases} \tag{7}$$

Using the complex vector, the stationary reference frame model is shown in Equation (8).

$$L\frac{di_{\alpha\beta}}{dt} = e_{\alpha\beta} - v_{\alpha\beta} - ri_{\alpha\beta} \tag{8}$$

Thus, the model could be transformed into the rotating $d-q$ synchronous frame by replacing "d/dt" with "d/dt+jω" as shown in Equation (9).

$$\left(\frac{d}{dt} + j\omega\right) Li_{dq} = e_{dq} - v_{dq} - ri_{dq} \tag{9}$$

The model can also be shown as

$$\frac{d}{dt} Li_{dq} = e_{dq} - v_{dq} - (r + j\omega L)i_{dq} \tag{10}$$

Transforming into the s domain, the model can be shown as

$$I_{dq} = (E_{dq} - V_{dq})\frac{1}{(j\omega L + r) + sL} = (E_{dq} - V_{dq})\frac{1}{L\left(\left(j\omega + \frac{r}{L}\right) + s\right)} \tag{11}$$

Equation (11), therefore in the synchronous reference frame, shows the plant has only one complex pole found at -r/L - $j\omega$. Hence, by choosing the proper parameters, the PI conventional controller would be zero, and approximately cancel the plant pole. In Equation (12) the controller is found as

$$C_{dq}(s) = \frac{K_p}{s}\left(\left(j\omega + \frac{K_i}{K_p}\right) + s\right) = K_p\frac{1}{s}\left(\left(j\omega + \frac{K_i}{K_p}\right) + 1\right) \tag{12}$$

Based on the complex vector perspective, the rectifier model transforms the single-input single-output (SISO) model as of the double-input double-output (DIDO) model. Figure 8 shows the block diagram of the obtained decoupling control.

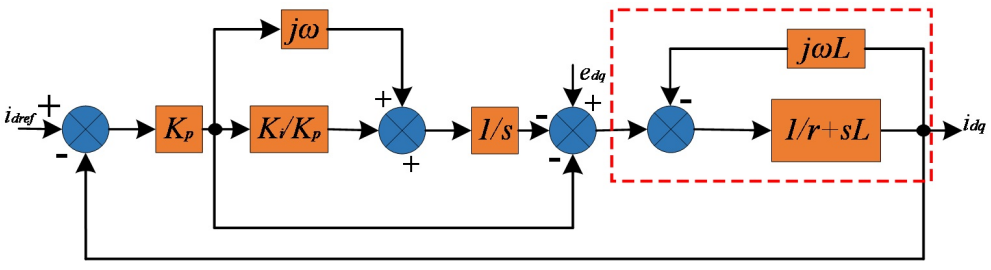


Figure 8. Complex vector decoupling control diagram.

It can be observed in Figure 8, without an exact and accurate value of inductance, that good performance could be attained. The K_i and K_p parameters can be selected by following the conventional PI controller.

$$j\omega + \frac{Ki}{Kp} = j\omega + \frac{r}{L} \tag{13}$$

Hence, $\frac{K_i}{K_p} = \frac{r}{L}$ by selecting proper value of K_p, and a proper cutoff frequency can be chosen, as mentioned in Table 1.

3.3. Design Outer Voltage Loop

In consonance with the power-balancing principle, avoiding the losses in the rectifier, we take

$$P_{ac} = P_{dc} \tag{14}$$

The active input power is

$$P_{ac} = v_{sa}i_{sa} + v_{sb}i_{sb} + v_{sc}i_{sc} \tag{15}$$

The equation in the synchronous $d-q$ reference frame turns into

$$P_{ac} = 1.5(v_{sd}i_{sd} + v_{sq}i_{sq}) \tag{16}$$

where v_{sk}, i_{sk} $(k = d, q)$ are reactive and active elements of the input current and voltage in the $d-q$ synchronous frame. The DC side power can be described as

$$P_{dc} = v_{dc}i_{dc} = v_{dc}C\frac{dv_{dc}}{dt} + \frac{v_{dc}^2}{R_L} \tag{17}$$

Equation (16) is equal to Equation (17), then

$$v_{dc}C\frac{dv_{dc}}{dt} + \frac{v_{dc}^2}{R_L} = 1.5(v_{sd}i_{sd} + v_{sq}i_{sq}) \tag{18}$$

From Equation (18), it can be seen that there are nonlinear items (i.e., the output voltage is squared, and it becomes a differential when multiplying the output voltage), which shows nonlinear relations among v_{dc} and i_{sq}, i_{sd}.

The d-axis is commonly put in the same direction as the voltage vector in the synchronous $d-q$ reference frame. If the maximum value of three-phase voltage is v_m, its symmetrical phase will be

$$\begin{cases} v_{sd} = V_m \\ v_{sq} = 0 \end{cases} \tag{19}$$

where $v_{sq} = 0$. Thus, the v_{dc} output voltage is calculated with only the variable i_{sd}, and there is nonlinear relation among them.

In this study, the outer voltage control loop, a control scheme in which the capacitor energy is treated as a variable, is discussed. As there is a linear relation between the active current and capacitor energy, the system has great control characteristics with a simple PI controller. First, we analyze and transform the rectifier voltage, as shown in Equation (18).

$$\frac{dv_{dc}^2}{dt} = 2v_{dc}\frac{dv_{dc}}{dt} \tag{20}$$

The equation will be

$$\frac{dv_{dc}^2}{dt} = -\frac{2}{R_LC}v_{dc}^2 + \frac{3}{c}v_{sd}i_{sd} + \frac{3}{c}v_{sq}i_{sq} \tag{21}$$

where

$$w_c = \frac{1}{2}Cv_d^2c \tag{22}$$

$$v_{dc}^2 = \frac{2W_c}{C} \tag{23}$$

Equation (21) will be

$$\frac{d}{dt}w_c = -\frac{2}{R_L C}w_c + 1.5V_{sd}i_{sd} + 1.5V_{sq}i_{sq} \tag{24}$$

If Equation (19) is put into Equation (24), then we obtain

$$\frac{d}{dt}w_c = 1.5V_m i_{sd} - \frac{2}{R_L C}w_c \tag{25}$$

Equations (22) and (23) define the capacitor output energy. If w_c, the capacitor energy, is considered as a new control variable, a linear relation will exist between i_{sd} and w_c, which is presented in Equation (25). The transformer function between the active current and capacitor current can be defined as

$$\frac{W_c(s)}{I_{sd}(s)} = \frac{1.5V_m}{\left(s + \frac{2}{R_L C}\right)} \tag{26}$$

Capacitor energy is considered as a variable, and in the outer loop a linear PI regulator is used. If the capacitor energy is defined as $W_{cref} = 1/2CV_{dcref}^2$ and the DC voltage reference is $vdcref$, the control system structure will be as shown in Figure 9.

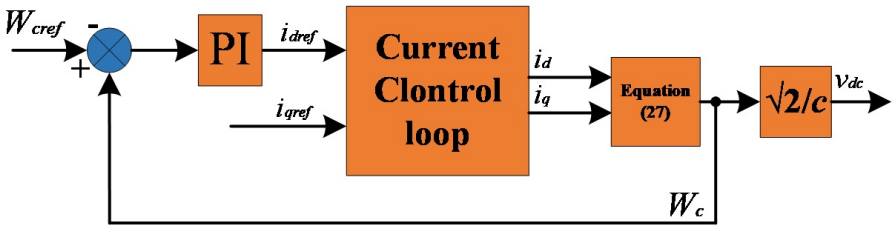


Figure 9. Capacitor energy as a variable control system.

The PI regulator transform function is described as

$$G_P I(s) = \frac{K_{Iv}}{S} + K_{pv} \tag{27}$$

While selecting the controller in the double-closed-loop control system, it can be assured that the bandwidth of the internal current loop is wider than that of the outer voltage loop when examining the outer voltage control loop. In addition, the responding behavior of the current is quick enough to ignore the delay.

The closed-transform function system is defined as

$$\frac{W_c(s)}{W_{cref}(s)} = 1.5V_m K_{Pv} \frac{S + \frac{K_{Iv}}{K_{Pv}}}{s^2 + \left(\frac{2}{R_L C} + \frac{3}{2}V_m K_{Iu}\right)s + 1.5V_m K_{Iv}} \tag{28}$$

It is observable that the closed-loop transform function of capacitor energy is a second-order linear system. When S→0, the gain function will be $W(s)/W_{ref}(s)\rightarrow 1$, with a step response, which shows that the capacitor's steady-state error and the steady-state error of the voltage are zero.

4. Simulation Results

To demonstrate the effectiveness and accuracy of the suggested control system for the DC–DC converter, simulations are carried out in MATLAB/Simulink software (MathWorks Inc, Natick, MA, USA), and parameters are specified in Table 1. First, on the HV side, the port (I) input DC voltage is a 20 kV waveform. Using the SVPWM technique, the line voltage modulation index is 0.8. After passing through the passive LC filter by reducing harmonics, the sinusoidal AC output of the 10 kV waveform is as shown in Figure 10. On the LV side, the port (III) input AC is 10 kV, and the line voltage, phase voltage and output constant 400 V are as shown in Figure 11. Figure 12 shows the different effects of loads when the load changes in parallel, and only 2.3% load variations will be accepted (according to IEEE standard, 5% variation is acceptable [44]). The output from port (II) 500 V variable output is shown in Figure 13, which changes according to load variation. Three-phase voltage and PQ are shown in Figure 14. The DC voltage waveform results are compared with [45]. We notice that the load changed from 50 Ω to 100 Ω at 0.14 s and is shown in Figure 15. The DC voltage reduced, there was a slight voltage dip, and then it tracked back to its original condition. It can be examined that the proposed topology is effective in conditions of uncertain load disturbances. The robustness of the suggested control system is proved, and the bidirectional power flow waveform for the current and voltage are clearly seen Figure 16. In Figure 17, the capacitor energy is shown as a variable. The simulation results show that the overshoot of the output voltage is reduced more than 70 V, so the control system has a superior performance.

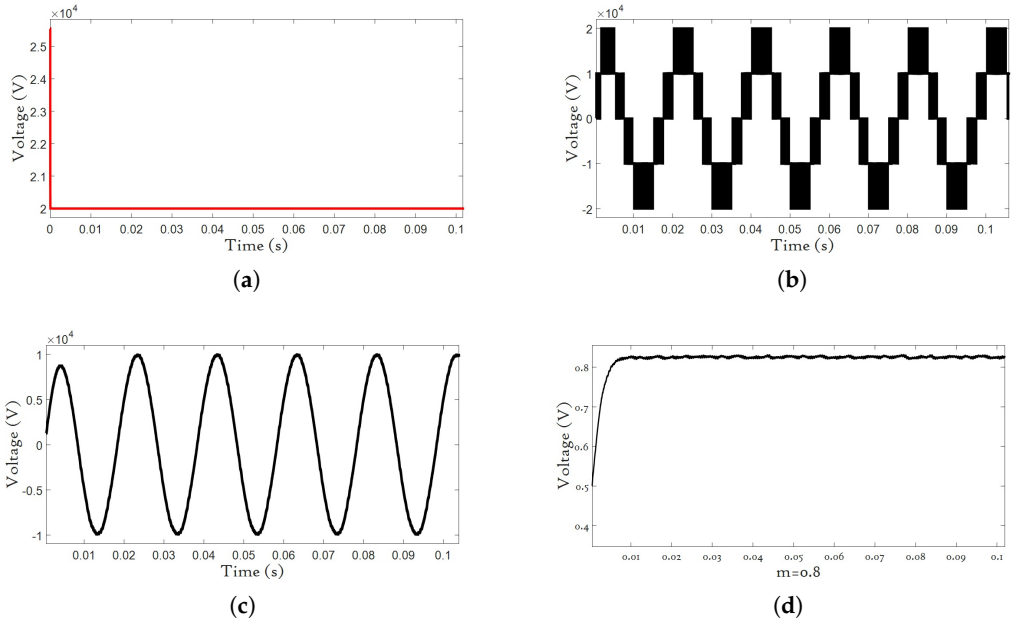


Figure 10. HV side: (**a**) Input DC voltage, (**b**) line voltage, (**c**) output AC and (**d**) modulation index 0.8.

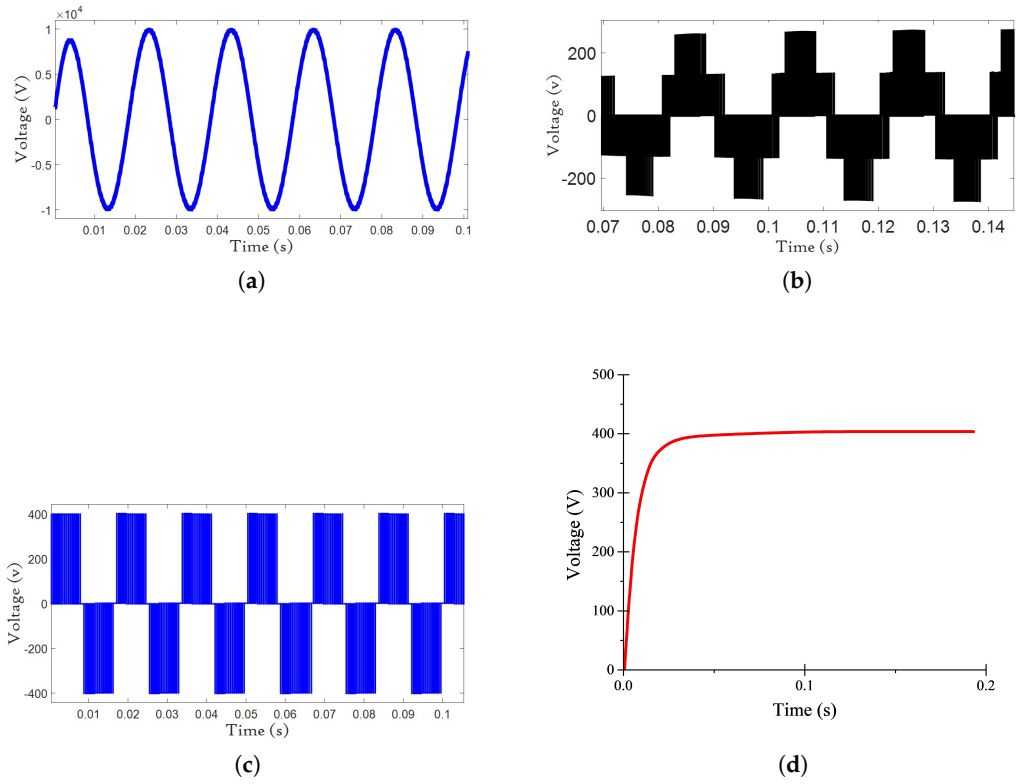


Figure 11. Port II: (**a**) input AC 10 kV, (**b**) line voltage (**c**), phase voltage and (**d**) output constant 400 V.

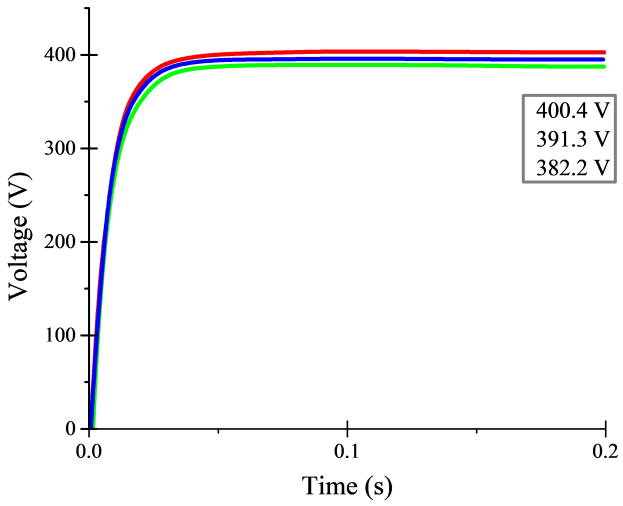


Figure 12. Effects of load variations.

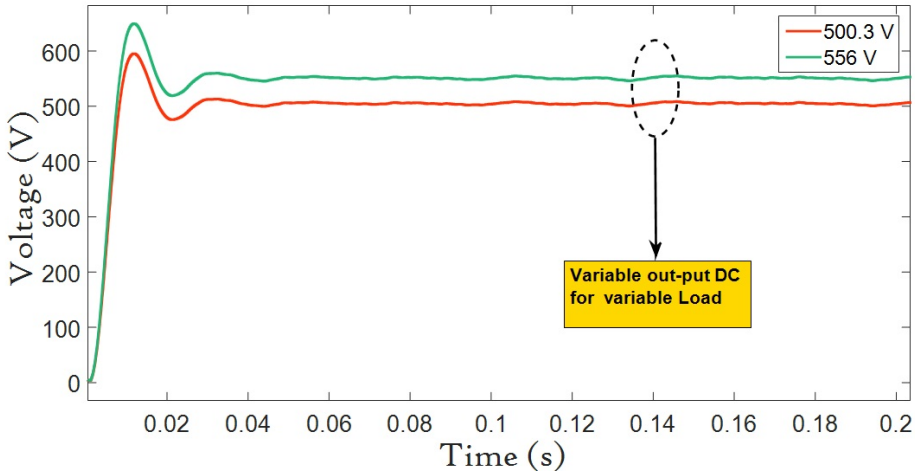
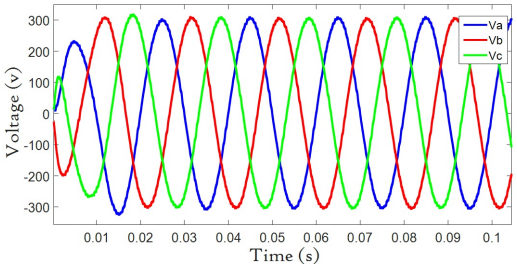
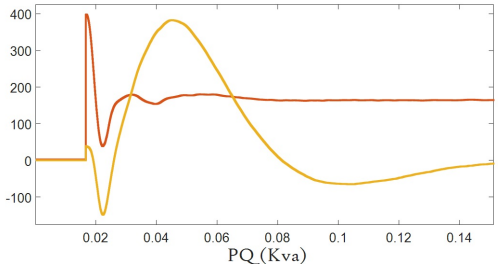


Figure 13. Port (II) 500 V variable output, which changes according to load variation.



(**a**)



(**b**)

Figure 14. (**a**) Three-phase voltage and (**b**) PQ.

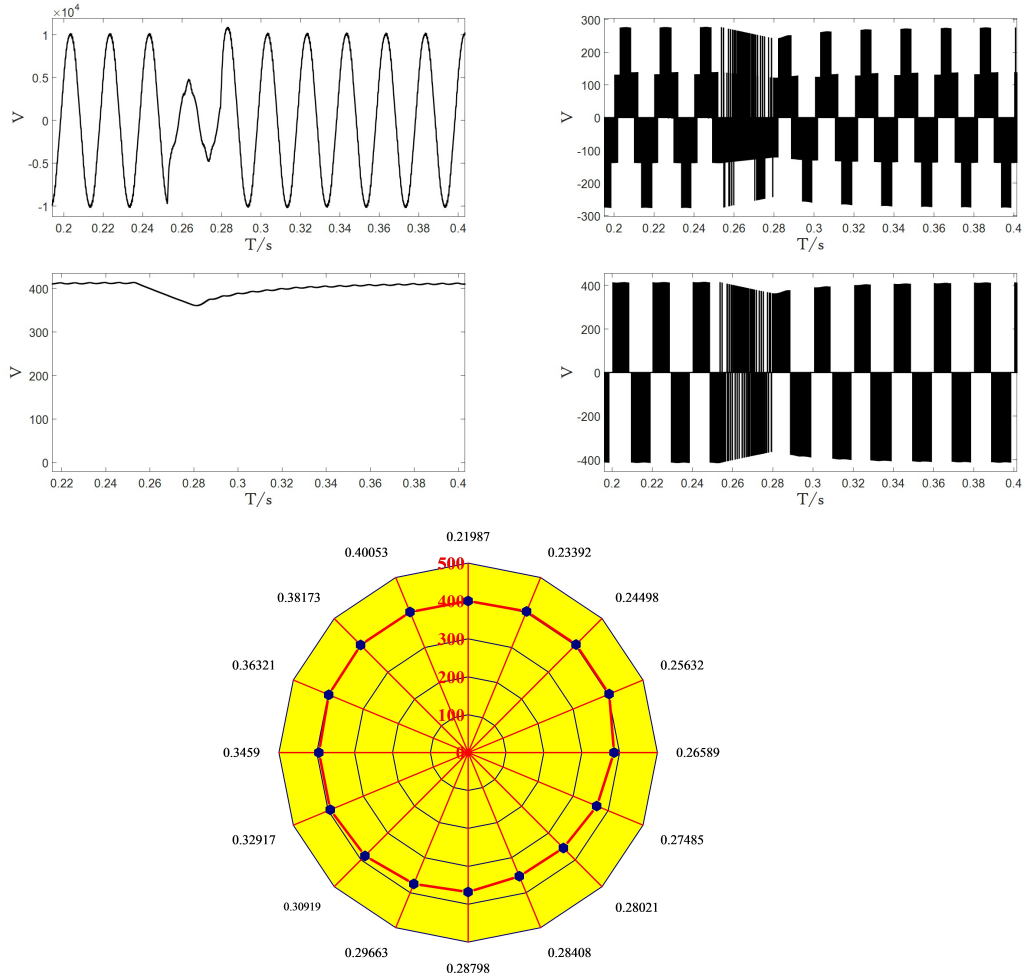


Figure 15. Response of the control system during load changes.

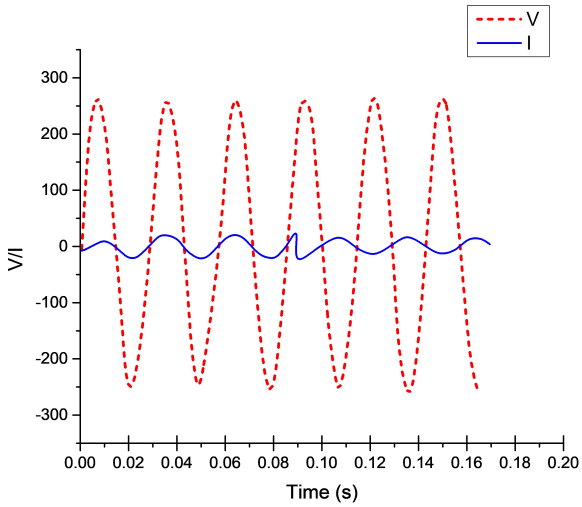
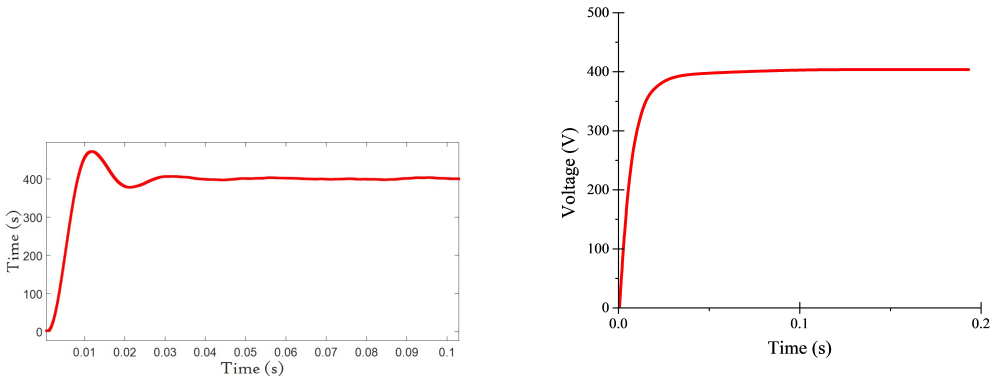


Figure 16. Bidirectional power flow waveform of the current and voltage.



(**a**) (**b**)

Figure 17. (**a**) Output voltage wave with conventional strategy and (**b**) output voltage with the presented control strategy.

5. DC–DC Converter Comparison Analysis

5.1. Devices Comparison and Analysis

A comparison study of semiconductor devices is shown in Table 2. The ratings are chosen according to how close the performances of the converters are to each other during operation at 400 V, 20 A and 150 °C, and key parameters are obtained from their respective datasheets.

Table 2. Parameters of Power Devices.

Device Parameters	SiC MOSFET	Si IGBT
Part number	C2M0080120D	NGTB20N120LWG
Manufacturer	Cree	On semi
Maximum rating	1200 V, 31.6 A	1200 V, 20 A
Maximum junction temperature	150	150
Thermal resistance	0.60	0.65
Voltage fall time	2.35×10^{-8}	1.2×10^{-7}
Voltage rise time	3.5×10^{-8}	4.0×10^{-8}
Drain current	36 A	20 A

Because of the higher breakdown voltage, low state resistance, much lower parasitic capacitance and higher switching frequency compared to Si, SiC technology minimizes losses and volume. In this section the semiconductor devices are compared, and conduction loss and switching loss, efficiency, wide range of switching frequencies, costs and overall performances are evaluated. The process life cycle is shown in Figure 18. An accurate mathematical model was developed to represent the DC–DC converter's overall performance, and loss was calculated using the equations in Appendix A under 75% and full-resistive load conditions. Datasheet extrapolations were used, and simulations were carried out in LTSpice software (Analog Devices, Norwood, Massachusetts, USA), where the SiC MOSFET model was created according to datasheet and manufacturer specifications.

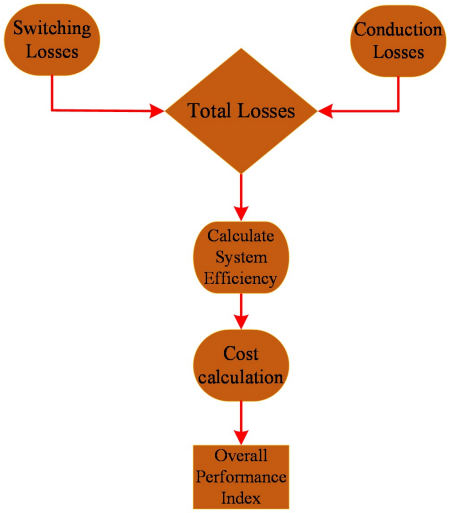


Figure 18. Performance evaluation chart.

5.2. Converter Performance at Variable Switching Frequencies

The total power loss (P_L) of the converter is acquired by the sum of switching losses (P_{sw}), conduction losses ($P_{conduction}$) and the capacitor inductor loss (P_{ic}). It can be obtained by the following equation:

$$P_L = P_{sw} + P_{conduction} + P_{ic} \tag{29}$$

Specifications of the DC–DC converter are presented in Table 3. The conduction and switching losses were calculated for V_{dc} = 400 V, P_{out} = 15 kW and R_{gate} = 10 Ω.

Table 3. Comparison between Si and WBG materials.

Properties	Si	4H-SiC
Band gap E_g [eV]	1.12	3.26
Breakdown electric field E_c [MV·cm^{-1}]	0.2	2.5
Intrinsic carrier concentration n_i cm^{-3}	1.5×10^{10}	8.2×10^{-9}
Holes mobility μ_P [cm^2·V^{-1}·s^{-1}]	420	115
Saturation velocity V_s [cm·s^{-1}]	1×10^7	2×10^7
Thermal conductivity λ [W·K cm·s^{-1}]	1.5	4.9

Conduction losses for every switching cycle were calculated, and loss created by the transistor junction temperature, on-resistance and transistor current were evaluated. The switching losses were determined based on turn-off and turn-on energy, transistor voltage, gate resistor, transistor current and junction temperature. According to the SiC MOSFET and Si IGBT transistor datasheets, reverse recovery energy is included during turn-off and turn-on phases. Hence, it is not compulsory to consider these losses independently. Energy stored in the output capacitance of the transistor was also included in the turn-off and turn-on energy states.

The total power losses are shown in Figures 19 and 20 at three junction temperatures of 25 °C, 100 °C and 150 °C when the switching frequency was increased from 10 to 100 kHz. The results reveal that SiC had lower losses in the considered switching frequency range at low junction temperatures. At high junction temperature, it is clearly seen in the diagrams that the total SiC losses were below total Si losses; hence, it is noteworthy that the influence of increased junction temperature on the total power losses in the SiC MOSFET-based converter was lower than that of Si IGBT due to the higher thermal conductivity of SiC materials.

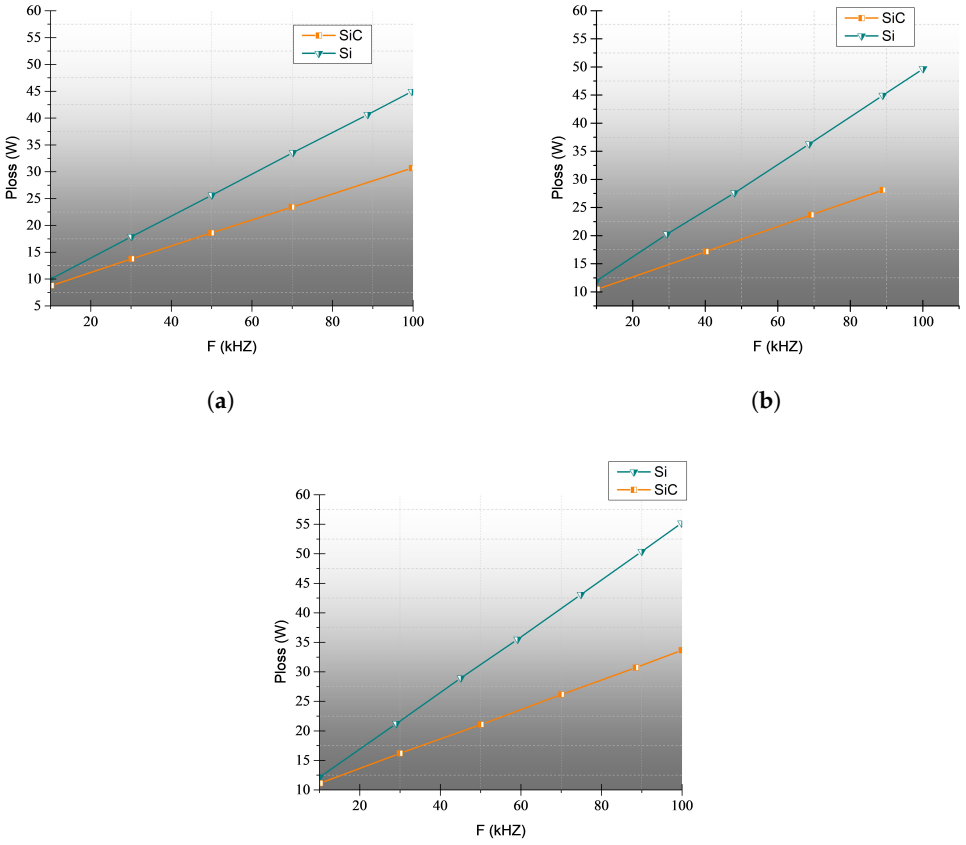


Figure 19. SiC and Si losses at (**a**) T = 25 °C, (**b**) T = 100 °C and (**c**) T= 150 °C.

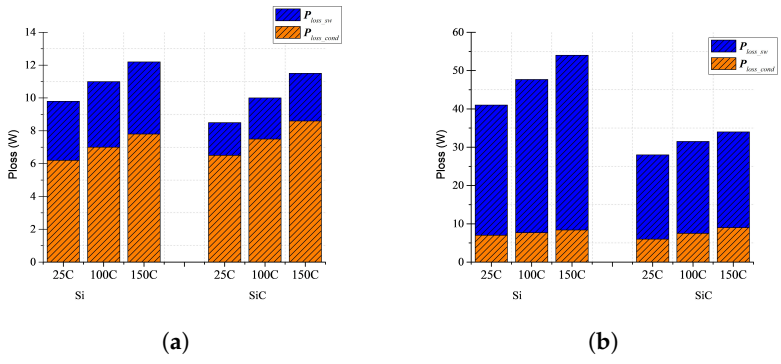


Figure 20. Switching and conduction losses at (**a**) F_{sw} = 10 kHz and (**b**) F_{sw} = 100 kHz.

5.3. Simulation and Analysis

Some specifications of the DC–DC converter are shown in Table 4. The specifications are chosen according to converter model.

Simulations were carried out in LTSpice software. The SiC MOSFET model from CREE (Research Triangle Park, North Carolina, United States) was created according to datasheet and manufacturer specifications. A mathematical model was developed to represent the converter's overall performance and loss calculations and by using the equations in Appendix A under 75% and full-resistive load conditions. The calculation results are shown in Figure 21 and Table 5.

Table 4. Converter specifications.

Specifications	Values
Low side voltage (V)	400 V
Power rating P (kW)	15
Switching frequency f (kHz)	20
Choke inductance (mH)	2
Junction temperature Tj (°C)	135
Equivalent series resistance for capacitor (mΩ)	4.5
Series resistance for inductor (Ω)	0.02
Load resistance (Ω)	100

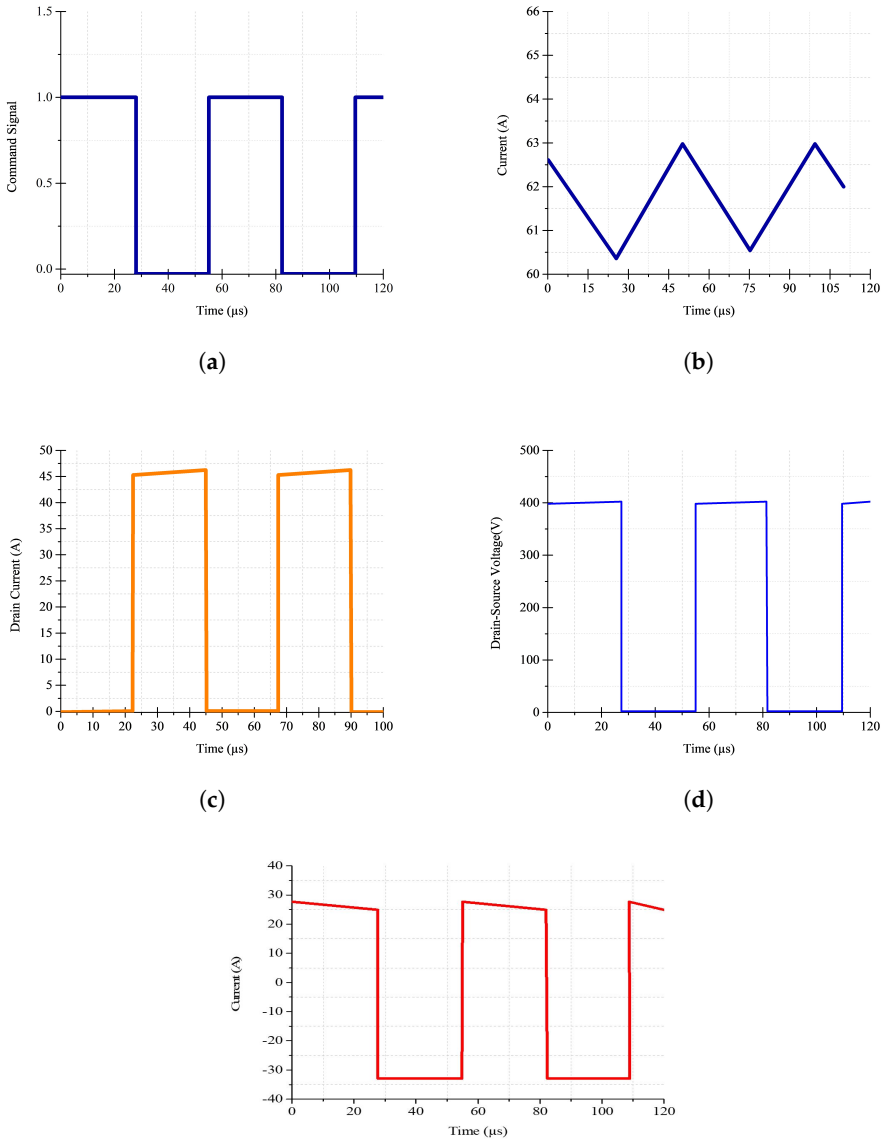
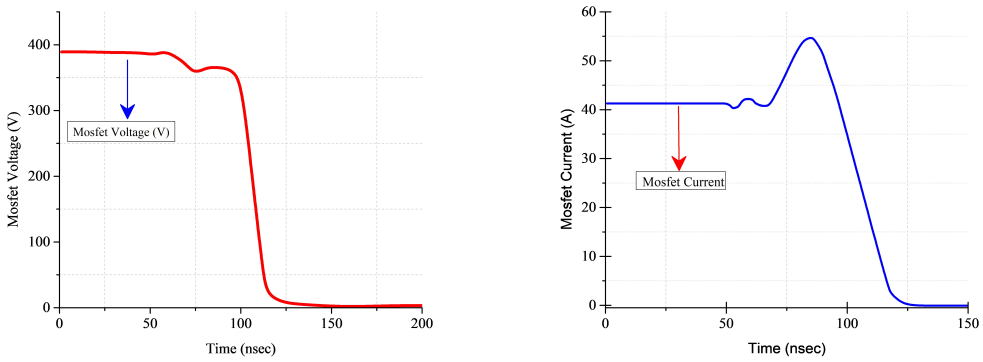


Figure 21. Key waveforms of SiC MOSFET (top to bottom: gate command signal, inductor ripple current, SiC drain current and voltage, and capacitor ripple current). (**a**) Gate signal, (**b**) inductor ripple current, (**c**) SiC MOSFET drain current, (**d**) drain voltage and (**e**) capacitor ripple current.

As it can be seen in Figure 21, the output voltage of the DC–DC converter was 397 V, with peak-to-peak ripple less than that 5 V. The average inductor current was 60 A, with 3 A peak-to-peak ripple current, which meets the low ripple current requirement. Since SiC MOSFET has small input capacitance, the gate driver is able to fully turn off and turn on the device faster than the Si MOSFET, as shown in Figure 22.



(**a**) (**b**)

Figure 22. Switching transients of the SiC converter simulation: (**a**) switching voltage and (**b**) current.

Table 5. Calculated efficiency and loss.

	Si IGBT	**SiC MOSFET**
Full Load		
Conduction Loss ($P_{conduction}$)	186.32	113.05
Switching Loss (P_{sw})	214.5	33.17
Inductor + Capacitor Loss (P_{ic})	31.175	30.78
Total Loss (P_L)	432	117
Converter Efficiency η (%)	**97.12**	**98.82**
75% Load		
Conduction Loss ($P_{conduction}$)	178.08	92.825
Switching Loss (P_{sw})	220.8	33.325
Inductor + Capacitor Loss (P_{ic})	19.625	17.85
Total Loss (P_L)	418	141
Converter Efficiency η (%)	**97.21**	**99.06**

The above mathematical results show that by using SiC devices, both switching and conduction losses decreased, which is expected according our prediction. It is notable that SiC MOSFET had a total switching loss (P_{sw}) of only 33 W at full and 30 W at 75% load, respectively, which is almost one-fifth of the total switching losses of Si IGBT. The conduction loss ($P_{conduction}$) of SiC MOSFET was also reduced 40–45% as compared to the Si design and capacitor and inductor losses (P_{ic}) are nearly the same because the component ESRs and root mean square (RMS) current values are same). The overall efficiency of the SiC design was 99.06% at full load and 98.82 for 75% load; it is 1.85% higher than that for all Si design models. From Figure 23 it is clearly seen that all three SiC portions (switching loss, conduction loss and capacitor loss) were superior; hence, for higher-frequency operations the SiC converter has a better potential for use than the Si.

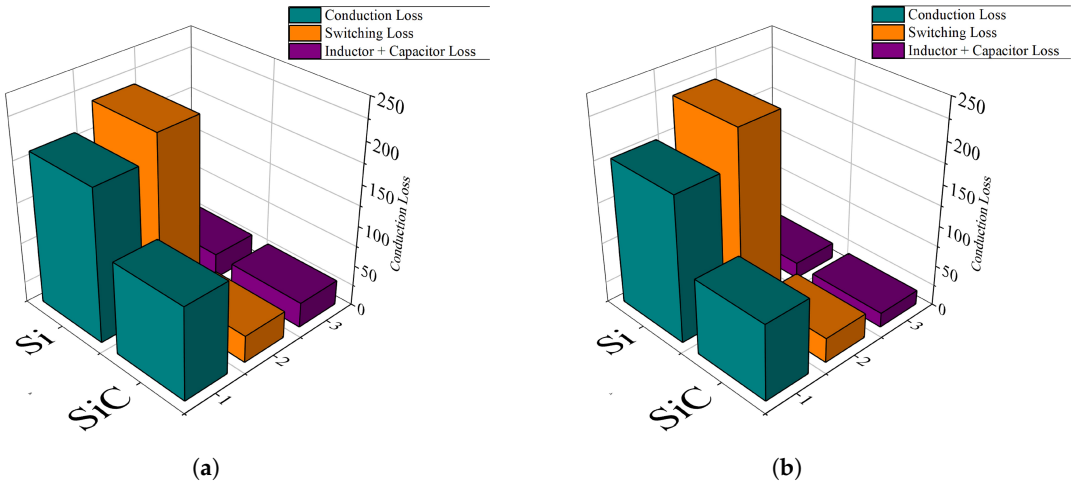


Figure 23. Loss comparisons at (**a**) 100% and (**b**) 75%.

In Figure 24, at 75% load the efficiency of the converter was slightly better than at full load; this is due to the current squared relationship, and the resistive loss components will drop down to 1/4 of the original value, while the resistance value will not change. In Table 5, capacitor and inductor loss (P_{ic}) exactly followed this rule, but conduction loss ($P_{conduction}$) did not. In the Si IGBT case, conduction losses were not purely resistive, but in the MOSFET case, conduction losses were resistive. Thus, conduction loss in the SiC MOSFET case were smaller compared to Si as the load decreased. Furthermore, the switching losses were also reduced as compared to full load. Other losses (gate driver power consumption) were not included, as efficiency would be affected if these losses were included.

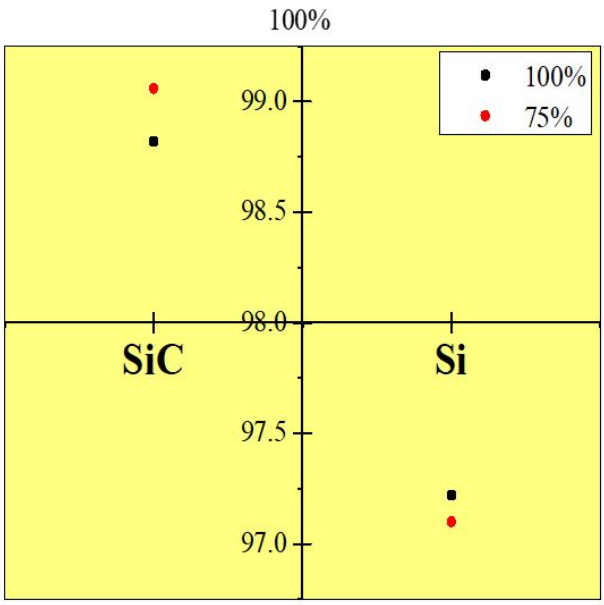


Figure 24. Efficiency comparison at 100% and 75% load.

6. Cost Comparison

In order to compare SiC and Si costs, running and initial prices were taken into account. The initial prices of SiC MOSFET (C2M0080120D) and Si IGBT (NGTB20N120LWG) devices, which are used in the converters, have been summarized in Table 6. All prices were taken from the Farnell (Leeds, UK) website on 29 Jan 2020, at 100 pieces. The heat sinks were also found on the Farnell website and chosen on the basis of temperature increases for the given power loss.

Table 6. Cost comparison.

	SiC MOSFET C2M0080120D	Si IGBT NGTB20N120LWG
Semiconductors	£ 436.00	£ 212.00
Heat sink	£ 223.11	£ 459.48
Drivers	£ 3640	£ 353.89

The costs of semiconductors are compared in Figure 25. It can be seen in Table 6 that the cost of SiC MOSFET was more than double that of Si IGBT because of the drivers cost. The drivers of SiC are expensive because a special driving scheme is needed to support the SiC. On the other hand, the cooling requirements for Si are much greater than for SiC; thus, the cost difference is not as big a barrier as one may have expected.

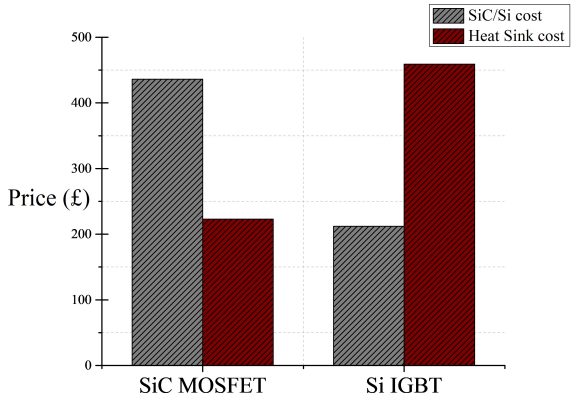


Figure 25. Cost comparison of Si and SiC devices.

7. Conclusions

A comprehensive performance study of a proposed MVDC DC–DC three-level converter has been presented. The suggested multi-port converter on the LV side provides two nominal voltages of 400 V (constant) and 500 V (variable), respectively. A novel and effective double-closed-loop control strategy on the LV side was analyzed in two scenarios. In a voltage control scheme, according to the investigation, the capacitor energy is analyzed as a variable, and the dynamic response of the output voltage is improved. An inner current loop control was also analyzed without an exact inductance value in complex vector frame. When designing the controllers, uncertain load disturbances during voltage dips were taken into account. The simulation results demonstrate that the fluctuations and voltage dips can be controlled effectively by applying the proposed control topology. Consequently, this topology is effective and applicable to enhance the robustness and energy conversation of a system. In the second portion, a comparison study between new SiC and Si semiconductor power devices is given. Test simulations for both devices were built and verified. The performance and operation of semiconductors were compared at different specifications, and conduction loss switching loss, wide range of switching frequencies, cost comparisons and overall performances were evaluated. The efficiency of the SiC-based converter was found above 99% under two resistive load conditions,

which shows the efficiency of the SiC-based converter is 1.85% higher than that of Si. SiC MOSFET can also operate at higher temperatures, and less cooling is required because of the decrease in device losses. Costs of both devices were compared. SiC drivers are expensive, but the cooling requirement for Si is much greater than that of SiC; thus, the cost difference is not a big barrier. The outcomes of this study are valid for all kinds of DC–DC converters used in numerous other applications. Therefore, this study is helpful to enhance the reliability, and improve the overall efficiency, of converters that can be derived in the future.

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Appendix A

Table 1: Devices loss calculation model.

Conduction losses—two-level converter

$$P_{c-T_1,T_2} = \frac{V_{o,T}\hat{I_L}}{2\pi}\left[1 + \frac{M\pi}{4}cos(\varphi)\right] + \frac{r_{0,T}\hat{I_L^2}}{2\pi}\left[\frac{\pi}{4} + \frac{2M}{3}cos(\varphi)\right] \tag{A1}$$

$$P_{c-D_1,D_2} = \frac{V_{o,D}\hat{I_L}}{2\pi}\left[1 - \frac{M\pi}{4}cos(\varphi)\right] + \frac{r_{0,D}\hat{I_L^2}}{2\pi}\left[\frac{\pi}{4} - \frac{2M}{3}cos(\varphi)\right] \tag{A2}$$

Switching losses—two-level converter

$$P_{s-T_1,T_2} = \frac{f_s}{\pi}(E_{on} + E_{off})\left(\frac{V_{dc}}{V_{ref}}\right)\left(\frac{\hat{I_L}}{I_{ref}}\right) \tag{A3}$$

$$P_{s-D_1,D_2} = \frac{f_s}{\pi}E_{rr}\left(\frac{V_{dc}}{V_{ref}}\right)\left(\frac{\hat{I_L}}{I_{ref}}\right) \tag{A4}$$

Conduction losses—three-level NPC

$$P_{c-T_1,T_4} = \frac{V_{o,T}M\hat{I_L}}{4\pi}[sin(\varphi) + (\pi - \varphi)cos(\varphi)] + \frac{r_{o,T}M\hat{I_L^2}}{4\pi}\left[\frac{8}{3}cos^4\left(\frac{\varphi}{2}\right)\right] \tag{A5}$$

$$P_{c-D_1,D_4} = \frac{V_{o,D}M\hat{I_L}}{4\pi}[sin(\varphi) - \varphi cos(\varphi)] + \frac{r_{o,D}M\hat{I_L^2}}{2}\left[\frac{4}{3\pi}sin^4\left(\frac{\varphi}{2}\right)\right] \tag{A6}$$

$$P_{c-T_2,T_3} = \frac{V_{o,D}\hat{I_L}}{\pi}\left[1 - \frac{M}{4}(sin(\varphi) - \varphi cos(\varphi))\right] + \frac{r_{o,T}\hat{I_L^2}}{4}\left[1 - \frac{8M}{3\pi}sin^4\left(\frac{\varphi}{2}\right)\right] \tag{A7}$$

$$P_{c-D_2,D_3} = \frac{V_{o,D}M\hat{I_L}}{4\pi}[sin(\varphi) - \varphi cos(\varphi)] + \frac{r_{o,D}M\hat{I_L^2}}{2}\left[\frac{4}{3\pi}sin^4\left(\frac{\varphi}{2}\right)\right] \tag{A8}$$

$$P_{c-D_5,D_6} = \frac{V_{o,D}\hat{I_L}}{\pi}\left[1 - \frac{M}{4}(2sin(\varphi) - (2\varphi - \pi)cos(\varphi))\right] + \frac{r_{o,D}\hat{I_L^2}}{4}\left[1 - \frac{4M}{3\pi}(1 + cos^2(\varphi))\right] \tag{A9}$$

Switching losses—three-level NPC

$$P_{s-T_1,T_4} = f_s(E_{on} + E_{off})\left(\frac{0.5V_{dc}}{V_{ref}}\right)\left(\frac{\hat{I_L}}{I_{ref}}\right)\left(\frac{1+cos(\varphi)}{2\pi}\right) \quad \text{(A10)}$$

$$P_{s-D_1,D_4} = f_s E_{rr}\left(\frac{0.5V_{dc}}{V_{ref}}\right)\left(\frac{\hat{I_L}}{I_{ref}}\right)\left(\frac{1-cos(\varphi)}{2\pi}\right) \quad \text{(A11)}$$

$$P_{s-T_2,T_3} = f_s(E_{on} + E_{off})\left(\frac{0.5V_{dc}}{V_{ref}}\right)\left(\frac{\hat{I_L}}{I_{ref}}\right)\left(\frac{1-cos(\varphi)}{2\pi}\right) \quad \text{(A12)}$$

$$P_{s-D_2,D_3} = 0 \quad \text{(A13)}$$

$$P_{s-D_5,D_6} = fE_{rr}\left(\frac{0.5V_{dc}}{V_{ref}}\right)\left(\frac{\hat{I}}{I_{ref}}\right)\left(\frac{1+cos(\varphi)}{2\pi}\right) \quad \text{(A14)}$$

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