 Simulation of Stress Distribution in the Silicon Substrate

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Introduction

Si oxidation technological process is common using in the semiconductors production process. The oxide, which is growing in thermal oxidation, causes intrinsic stresses in all structure.

In stress, area might be arising dislocations. If it use integrated elements isolation methods such as LOCOS and oxidized trench, thin film deposition in different temperature it’ll appear various intrinsic stresses, which increases defects.

By using mathematical simulation program ATHENA was performed mathematical simulation of Si thermal oxidation and thin films deposition technological processes, and was evaluated the distribution of stresses in all semiconductor structure.

Stress calculation model in the growing oxide

The fabrication of integrated circuit microelectronic structures and devices vitally depends on the thermal oxidation process for the formation of gate dielectrics, device isolation regions, spacer regions, and the ion implantation masks regions. Particularly, the precise controls of silicon dioxide thickness as device geometries continue to scale to nano-dimensions [1].

The Viscous Model calculates stresses in the growing oxide and creates almost the same shape for the silicon oxide interface, as does the Compress model. The stresses in the oxide are calculated as follows:

\[ \sigma_{xx} + \sigma_{yy} = \frac{2 \cdot VISC.0 \cdot \exp \left( \frac{VISC.E}{kT} \right)}{1 - 2 \cdot POISS.R} \times \left( \frac{\partial v_x}{\partial x} + \frac{\partial v_y}{\partial y} \right) \]  \hspace{1cm} (1)

\[ \sigma_{xx} - \sigma_{yy} = 2 \cdot VISC.0 \cdot \exp \left( \frac{VISC.E}{kT} \right) \times \left( \frac{\partial v_x}{\partial x} - \frac{\partial v_y}{\partial y} \right) \]  \hspace{1cm} (2)

where \( v_x \) and \( v_y \) are the x and y components of flow velocity \( v \) respectively. \( VISC.0 \) and \( VISC.E \) are the pre-exponential and activation energy, respectively for viscosity.

The stress-dependent nonlinear model based on Eyring’s work allows a description of the real shape of LOCOS profiles with kinks on the interface. Using equations 1, 2 and 3, the non-linear solver first finds a linear solution for flow velocities and stresses and then uses the stresses obtained to calculate the reduction factors for oxidant diffusivity, \( D_{eff} \), oxide viscosity, \( \mu \), and the interface reaction rate constant \( k \) as follows:

\[ D_{eff}^{(i)} = D_{eff}^{(i-1)} \cdot \exp \left( \frac{V_{d} (\sigma_{xx} + \sigma_{yy})}{kT} \right) \]  \hspace{1cm} (4)

\[ \mu^{(i)} = \mu^{(i-1)} \cdot \frac{\left( V_{r} V_{c} / \tau \right)}{2kT} \]  \hspace{1cm} (5)

\[ k^{(i)} = k^{(i-1)} \cdot \exp \left( \frac{-\sigma_{xx} V_{r} + \sigma_{yy} V_{c}}{kT} \right) \]  \hspace{1cm} (6)

where \( i \) is the iteration \( V_d, V_c, V_r \), and \( V_t \) are the activation volumes. \( \tau \) is the total shear stress:

\[ \tau = \frac{1}{2} \sqrt{\left( \sigma_{xx} - \sigma_{yy} \right)^2 + 4\sigma_{xy}^2} \]  \hspace{1cm} (7)

\( \sigma_r \) is the normal component of the total stress:

\[ \sigma_r = \sigma_{xx} n_x^2 + \sigma_{yy} n_y^2 + 2\sigma_{xy} n_x n_y \]  \hspace{1cm} (8)
\( \sigma_t \) is the tangential component of the total stress:

\[
\sigma_t = \sigma_{xx} n_x^2 + \sigma_{yy} n_y^2 + 2\sigma_{xy} n_x n_y;
\]  

(9)

where \( n_x \) and \( n_y \) are the \( x \) and \( y \) components of the unit vector normal respectively [2].

**Stress calculation models**

There are three ways to calculate stresses generated during semiconductor processing:

1. The first way is to calculate the stresses during viscous oxidation or viscous material reflow.
2. The second way is to calculate the stresses due to thin film intrinsic stress of thermal mismatch.
3. The third way is to follow stress history.

In the cases of the second and third methods, performing a finite element analysis of the material structure solving the similar set of equations as in the case of viscous oxidation. The only difference is the thermal expansion and intrinsic terms added to the right-hand side of equation 1:

\[
\sigma_{xx} + \sigma_{yy} - \frac{4(1 + \text{POISS.R})}{1 - 2 \cdot \text{POISS.R}} \times \exp\left(\frac{-\text{VISC.E}}{K T}\right) \times LCTE + \text{INTRIN.SIG} \times T.
\]  

(10)

The linear coefficient of the material thermal expansion \( LCTE \) can be specified as a function of temperature \( T \). The film intrinsic stress parameter \( \text{INTRIN.SIG} \) \( T_1 \) and \( T_2 \) are initial and final temperatures.

If the stress history method is specified, then calculates stresses when the simulation structure changes after etching, deposition, epitaxy, and diffusion processes. The temperature specified for current process step is used in the calculation. The final stress from the previous step is used as a initial condition for the subsequent step [2].

**Simulation of stress distribution**

Using mathematical simulation program ATHENA [3] was performed mathematical simulation of planar silicon surface oxidation (Fig. 1, 2, 3). Analyzing stresses in XX plane was observed that biggest stress \( \sim 4 \cdot 10^{18} \) dyne/cm\(^2\) generating in new formed SiO\(_2\) layer. The dyne is a unit of force specified in the centimeter-gram-second. In YY plane lower stress \( \sim 4 \cdot 10^{11} \) dyne/cm\(^2\) distribute in all structure, because the newly formed oxide easy lifts up the previously formed oxide. Since the surface of the oxide is not constrained, the oxide is free to move in this direction so negligible stress is induced normal to the Si-SiO\(_2\) interface.

Stress distribution in Si substrate also depends on crystallographic orientation. There were made the oxidation process’s mathematical simulation of Si substrates of 100, 110 and 111 crystallographic orientation.

By comparison mathematical simulation results (in figures 1, 2 and 3) was observed when Si substrate crystallographic orientation is 111 the stresses distribution is more equal.

Fig. 1. Stress distribution after planar Si wet oxidation: Si crystallographic orientation – 100; oxidation time – 10 min, temperature – 1000 ºC; a) – stress distribution in XX plane, b) - stress distribution in YY plane

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In non-planar regions such as convex and concave corners of silicon, a strain exerted in the silicon dioxide and in all structure. Silicon step thermal oxidation is modelled by using mathematical simulation program ATHENA (Fig. 4).

As seen in simulation results the growing oxide starts to crush in the internal corners. In this regions forming stresses $\sim 2.6 \cdot 10^{17}$ dyne/cm$^2$ because growing silicon oxide expanding perpendicular to the surface and expanding to the both sides. By analyzing stresses distribution in XX and YY planes the compressing stresses are biggest in the internal corners. This type of stresses appearing in SiO$_2$ and spreads to Si crystal.

As shown in figure 4 stress distributions in XX and YY planes, growing SiO$_2$ causes stretch effect at Si convex corners, which can arise to $\sim -2 \cdot 10^{18}$ dyne/cm$^2$. Therefore, when oxidizing the silicon of complex surface various character stresses arise in all structure. They can change physical properties of materials and can generate defects or damage all structure (Fig. 5).

The experimental results of silicon oxidation represented in figure 5 [4]. The dark areas show the stress and dislocations in the silicon structure. As we see the defects depends on SiO$_2$ thickness and on oxidation process temperature.

Fig. 2. Stress distribution after planar Si wet oxidation: Si crystallographic orientation – 110; oxidation time – 10 min, temperature – 1000 ºC; a) – stress distribution in XX plane, b) - stress distribution in YY plane

Fig. 3. Stress distribution after planar Si wet oxidation: Si crystallographic orientation – 111; oxidation time – 10 min, temperature – 1000 ºC; a – stress distribution in XX plane, b) - stress distribution in YY plane

Fig. 4. Stress distribution after Si uneven surface wet oxidation: oxidation time – 10 min, temperature – 1000 ºC; a) – stress distribution in XX plane, b) - stress distribution in YY plane

Fig. 5. Experimental results of silicon oxidation.
Local oxidation of silicon (LOCOS) is generally using in microelectronics. LOCOS oxide is using to isolate one integrated elements from another [1, 5, 6]. In this technology thermal silicon oxidation is using also. The main problem is that growing oxide move under Si3N4 film that rising from the substrate due to generated stress. In this case, the exposed surface become uneven and the defects can occur in protective Si3N4 film. Mathematical simulation of LOCOS oxidation performed using mathematical simulation program ATHENA. Stresses distributions in XX and YY planes analyzed in accordance with mathematical simulation results (Fig. 6).

The mathematical simulation results demonstrate that the stresses in XX and YY planes distribute in all structure irregular. The stress in growing silicon oxide extends to nearest areas and to thin films. In this case, stress distribution depends on Si3N4 film elasticity. Figure 6 demonstrate that stress is expanding in all structure by growing LOCOS oxide.

The biggest compression (~ 2.6·10^{17} dyne/cm^2) occurs then SiO2 lean against Si3N4 film edges (Fig. 6). It can point up that the biggest stresses occur in the corners of the structure. The stresses and grown SiO2 form depends on the elasticity of Si3N4 film. If Si3N4 film elasticity decreasing, newly forming SiO2 must take higher resistant force of Si3N4 film. Therefore stresses increasing in SiO2 layer and in all structure. Dislocations occur then stress reach critical material elasticity.

Trenches are popular isolation technologies that also exhibit dislocation generation problems [7]. By using mathematical simulation program ATHENA it was performed simulation of Si trenches oxidation technological operation.

Mathematical simulation results of ion plasma etched trench oxidation represented in figure 7. By analyzing stresses distribution in XX and YY planes was observed that forms wide range of stresses: compression and stretch. Stress distribute deep in all structure. In this case growing silicon oxide move under Si3N4 film therefore occur additional stress in SiO2 and Si3N4 layers. Very high stress occurs due to trench internal corners then horizontal and vertical growing oxide starting to crush. In first stress appear in silicon oxide layer and distribute to neighbouring regions later. Growing SiO2 thickness expanding stress as it shown in figure 7.
Rectangular trench form is forming by plasma-etched technology. This form has a couple internal and external corners. Therefore, very different stresses are generating. The structure can crash due to these stresses. To reduce stresses need to reduce the number of corners.

Mathematical simulation of thin film deposition process results presented at figure 8.

These simulation results show that the stresses in the Si substrate and thin film arising from nitride layer, which has an intrinsic stress of $\sim 2.88 \times 10^8$ dyn/cm$^2$ when deposited uniformly. This is thermal mismatch stress in the whole structure as the results of the temperature change.

Conclusions

1. After oxidation of the silicon of complex surface various character stresses arise in all structure. Observed, that growing oxide causes intrinsic stresses in all structure during thermal oxidation. They can change physical properties of the materials and can generate defects or damage all structure.

2. The lower stresses appear in planar regions. The bigger stresses appear in non planar regions. Growing SiO$_2$ causes stretch effect at Si convex corners, which can arise to $\sim -2 \times 10^{18}$ dyn/cm$^2$. The growing oxide starts to crush in the internal corners. In this regions forming stresses $\sim 4 \times 10^{18}$ dyn/cm$^2$. This type of stress appearing in SiO$_2$ and spreads to Si crystal.

3. Analyzing stresses distribution after planar silicon surface oxidation in XX plane it was observed that biggest stress $\sim 4 \times 10^{18}$ dyn/cm$^2$ generating in new formed SiO$_2$ layer. In YY plane lower stress $\sim 4 \times 10^{11}$ dyn/cm$^2$ distribute in all structure.

4. Stress distribution in Si substrate also depends on crystallographic orientation. It was observed when Si substrate crystallographic orientation is 111 the stresses distribution is more equal.

5. After LOCOS oxidation, the stresses distribute in all structure irregular. Stress distribution depends to Si$_3$N$_4$ film elasticity. The biggest compression ($\sim 2.6 \times 10^{17}$ dyn/cm$^2$) occurs then SiO$_2$ lean against Si$_3$N$_4$ film edges. Dislocations occur then stress reach critical material elasticity.

6. Thin film deposition also generates the stresses in all structure. These stress arising due to different thermal expansion coefficient of the silicon substrate ant Si$_3$N$_4$ thin film.
References


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Si oxidation technological process is common occurrence in the semiconductors production process. The oxide which is growing in thermal oxidation creates intrinsic stresses in all structure. In stress area might be arising dislocations. Various intrinsic stresses appear when using integrated elements isolation methods such as LOCOS and oxidized trench. Thin films such as silicon nitride, silicon oxide and polysilicon are mostly usable in the semiconductor production. These films have the intrinsic stresses, which appear in the films deposition process apropos of different thermal expansion coefficients of the materials. By using mathematical simulation program ATHENA was accomplished mathematical simulation of Si thermal oxidation and thin film deposition technological processes and was evaluated the distribution of stresses in all semiconductor structure, Ill. 8, bibl. 7 (in English; summaries in English, Russian and Lithuanian).


Для изготовления полупроводниковых приборов чаще всего используется технологический процесс окисления кремния. Во время окислительного процесса возрастающий окисел создает натяжение во всей структуре. В натянутых местах создается вероятность появления дислокаций. Самые разные натяжения создают, используя LOCOS и окисление углубления кремния - изолирующие методы интегральных элементов. Для изготовления полупроводниковых приборов также используются тонкие плёнки: Si₃N₄, SiO₂. Эти плёнки имеют внутренние натяжения, которые возникают во время нанесения плёнок. Натяжения возникают из-за разных коэффициентов температурного расширения материалов. Используя программу математического моделирования ATHENA, было произведено моделирование технологических процессов: окисление кремния и нанесение тонких плёнок. Произведён анализ распределения натяжений во всей структуре. Ил. 8, библ. 7 (на английском языке; рефераты на английском, русском и литовском языках).


Плоскидийных гамбос процесе даузай тайкoms Si oksidavimo technologinis procesas. Terminės oksidacijos metu augantis oksidas sukela vidinius įtempius visoje struktūroje. Įtempių vietose atsiranda galimybė susidaryti dislokacijoms. Įvairūs vidiniai įtempiai atsiranda ir taikant įtvarinio grando izoliavimo metodus, tokius kaip LOCOS ir oksiduotas griovelis. Plonas plėvelės, tokios kaip silicio nitradas, silicio oksidas ir polisilikis, dažniausiai yra naudojamos plusoininkinių gamyboje. Šios plėvelės turi vidinius įtempiai, kurie atsiranda plėvelių sudarymo metu dėl skirtinų medžiagų temperatūrinių plėtimosi koeficientų. Pasinaudojus matematiniu modeliavimo programa ATHENA atliktas Si terminės oksidacijos ir plonų plėvelių sudarymo technologinių procesų matematinis modeliavimas, atsižvelgiant įtempių pasiskirstymą visoje plusaininkio struktūroje, Ил. 8, библ. 7. (англ. kalba; santraukos anglų, rusų ir lietuvių k.).