Introduction

Bipolar technology has been used in a wide range of processing and communications area. However, low cost of CMOS technology has replaced bipolar technology. CMOS technology was started off by complementing bipolar technology in the entry and mid-range systems. CMOS technology uses only energy when signals change, thus reducing operating and cooling requirements by more than 50% compared with conventional bipolar technology. Lower power consumption means less cost. Neighboring element isolation is significant point of cumulative integration degree in CMOS technology [1].

Thermal oxidation is one of various methods used for neighboring element isolation. During thermal oxidation silicon forms a perfect oxide – SiO₂. Silicon dioxide [2] is a high-quality electrical insulator and can be used as a barrier material during impurity implants or diffusion, for electrical isolation of semiconductor device technology, as a component in MOS/CMOS structures, or as an interlayer dielectric in multilevel metallization structures such as multichip modules [3].

In MOS/CMOS structures regions between the active elements must be isolated [4]. LOCOS (Local Oxidation of Silicon), PBL (Poly-Buffered LOCOS), SWAMI (Side Wall Masked Isolation) technologies are composite isolation methods, which are formed using thermal oxidation [5].

The main purpose of this paper is to analyze stress, which appears during thermal oxidation in mentioned above micro and nano scales technologies. Using thermal oxidation conversion of micro scale into nano scale isn’t the same as reducing structures dimensions and technological parameters N times if integration degree of integrated circuit (IC) is N in these technologies.

Thermal oxidation

The formation of SiO₂ on a silicon surface is most often accomplished through a process called thermal oxidation. Thermal oxidation is a technique that uses extremely high temperatures (usually between 700 – 1300 °C) to promote the growth rate of oxide layers.

The oxide thickness is an important parameter for the oxidation process. Oxide growth rate is affected by time, temperature, and pressure. Oxide growth is accelerated by an increase in oxidation time, oxidation temperature or oxidation pressure. Other factors that affect thermal oxidation growth rate for SiO₂ are: the wafer's doping level, the presence of halogen impurities in the gas phase, the presence of plasma during growth and the presence of a photon flux during growth, the crystallographic orientation of the wafer.

There are two types of the thermal oxidation of SiO₂. This type depends on which oxidant type is used (O₂ or H₂O):

1. Dry oxidation (the oxidant is O₂):

   \[ Si_2(solid) + O_2(vapor) = SiO_2(solid). \]  

2. Wet oxidation (the oxidant is H₂O):

   \[ Si_2(solid) + 2H_2O(vapor) = SiO_2(solid) + 2H_2. \]  

Due to the relationships in these reactions and the difference between the densities of silicon and silicon oxide, approximately 44% of the silicon surface is "consumed" during oxidation [6]. For every 100 nm of SiO₂ growth, about 44 nm of silicon is “consumed” (Fig. 1).

Fig. 1. Thermal oxidation

\[
\text{Thickness of } Si \quad \text{Molar volume of } Si \quad \text{Thickness of } SiO_2 \quad \text{Molar volume of } SiO_2
\]

\[
\frac{\text{Thickness of } Si}{\text{Thickness of } SiO_2} = \frac{\text{Molar volume (Si)}}{\text{Molar volume (SiO}_2)}
\]
The growth of silicon oxide is the reaction of surface only – after the SiO₂ thickness begins to build up, the arriving oxygen molecules must diffuse through the growing silicon dioxide layer to get to the silicon surface in order to react. As a result, the chemical reaction occurs at the Si – SiO₂ surface.

Silicon thermal oxidation process consists of:
1. the diffusion of oxidant species through the silicon dioxide;
2. the reaction of Si and O₂ at the Si/SiO₂ interface that consumes silicon and generates new silicon dioxide;
3. the deformation of the entire structure to comply with the new geometry changes.

The Deal-Grove model

The Deal-Grove model of oxidation is used for the oxide growth kinetics. This model is generally valid for temperatures between 700 ºC and 1300 ºC, partial pressures between 0,2 and 1,0 atmospheres, and oxide thicknesses between 25 and 2000 nm for both wet and dry oxidation. Oxides thicker than 1000 nm require long exposures to very high temperatures and this will lead to oxidation.

In general case the growing silicon oxide thickness has following curve form (Fig. 2).

\[ X_{ox} = \frac{HkT}{N_i(1 + \frac{k_s}{h} + \frac{k_s}{D}t_{ox})}, \]  
\[ X_{ox}^2 = Bt_{ox}, \]  
where \( X_{ox} \) – the thickness of the growing oxide; \( B \) – the parabolic rate constant, \( t_{ox} \) – the oxidation time.

This formula shows that the oxide thickness grown is proportional to the square root of the oxidizing time, which means that the oxide growth is disturbed as the oxide thickness increase. This is because the oxidizing fractions have to travel a greater distance to the Si – SiO₂ interface as the oxide layer thickens.

If oxidation processes have very short durations then it maybe modeled by the Linear Growth law:

\[ X_{ox} = C(t_{ox} + \tau), \]  
where \( X_{ox} \) – the thickness of the growing oxide; \( C \) – the linear rate constant; \( t_{ox} \) – the oxidation time; \( \tau \) – the initial time displacement to account for the formation of the initial oxide layer at the start of the oxidation process.

Process simulation

Thermal oxidation process is simulated with ATHENA. ATHENA is a simulator that provides general capabilities for numerical, physically – based, two – dimensional simulation of semiconductor processing. Oxidation takes place when there is an interface between silicon (or polysilicon) and silicon dioxide or a silicon (polysilicon) surface is exposed to an oxidizing ambient. ATHENA simulates polysilicon oxidation in a very similar manner as silicon (almost all oxidation parameters for polysilicon are the same as for silicon). ATHENA also allows oxidation completely through a silicon (polysilicon) layer. This is a very important in processes (e.g., PBL) where polysilicon regions are completely consumed during oxidation. Exposed silicon surfaces usually have a thin native oxide layer, that’s why ATHENA automatically deposits a thin native oxide layer on all exposed silicon (polysilicon) surfaces at the beginning of oxidation steps.

Oxide and nitride is as viscous flow. Oxidation process is running in water steam. Thermal oxidation process in ATHENA is based on the linear-parabolic theory of Deal and Grove model. In micro scale simulated structures are shown in Fig. 3 – 5.

Lateral oxidation can take place in LOCOS structure during thermal oxidation. In this way lateral encroachment (bird’s beak) is created. Stress and dislocations less or more are created in all structures during oxidation. As see in Fig. 3 stress and defects is situated in silicon nitride, only small area of silicon oxide is defected. The main problem of this structure is that defects are situated in gate zone, where impurity and defects form voltage puncture, dielectric permittivity and others instabilities [1]. Push and pull forces are created in simulated structures:
**Fig. 3.** Stress XY in Local Oxidation of Silicon in micro scale (t=120 min., T=1000 ºC, SiO2=20 nm, Si3N4=150 nm, σ\(_{xy\text{ max}}\) = 3,59·10\(^{10}\) dyne/cm\(^2\), σ\(_{xy\text{ struct}}\) = 2,89·10\(^9\) dyne/cm\(^2\))

**Fig. 4.** Stress XY in Poly-Buffered Local Oxidation of Silicon in micro scale (t=120 min., T=1000 ºC, SiO2=20 nm, poly Si=100 nm, Si3N4=150 nm, σ\(_{xy\text{ max}}\) = 6,05·10\(^{11}\) dyne/cm\(^2\), σ\(_{xy\text{ struct}}\) = 1,97·10\(^{11}\) dyne/cm\(^2\))

**Fig. 5.** Stress XY in Side Wall Masked Isolation in micro scale (t1=4 min., t2=500 min., T=1000 ºC, SiO2=40 nm, Si3N4(1)\(^{st}\)=160 nm, Si3N4(2)\(^{nd}\)=40 nm, σ\(_{xy\text{ max}}\) = 1,45·10\(^{10}\) dyne/cm\(^2\), σ\(_{xy\text{ struct}}\) = -9,77·10\(^8\) dyne/cm\(^2\))

Thermally grown SiO\(_2\) is under compressive stress and as a result reduces the substrate forces exerted by the patterned Si3N4 film. In addition, significant stress relaxation occurs in the LOCOS structure due to the viscoelastic properties of the oxide, σ\(_{xy\text{ max}}\) = 3,59·10\(^{10}\) dyne/cm\(^2\), σ\(_{xy\text{ struct}}\) = 2,89·10\(^9\) dyne/cm\(^2\). In PBL picture (Fig. 4) a polysilicon layer is inserted between the pad oxide and the Si3N4 layer. In this case the purpose of the polysilicon is to provide relief of the stress that builds up during the oxidation. During thermal oxidation (Fig. 4) the stress zone is very small (σ\(_{xy\text{ max}}\) = 1,45·10\(^{10}\) dyne/cm\(^2\), σ\(_{xy\text{ struct}}\) = -9,77·10\(^8\) dyne/cm\(^2\)), the gate zone is not modified. But the deposition conditions of the polysilicon play a very important role in the stress-relief process and lead to extensive defect formation. PBL structure is prone to substrate pitting during polysilicon removal and these two effects can cause severe gate-oxide reliability problems. That’s why the Side Wall Masked Isolation is created. Lots of problems can be alleviated by using the SWAMI isolation structure. After thermal oxidation a low substrate defect density is created. In this structure σ\(_{xy\text{ max}}\) = 1,45·10\(^{10}\) dyne/cm\(^2\), σ\(_{xy\text{ struct}}\) = -9,77·10\(^8\) dyne/cm\(^2\). There is no polysilicon, which cause gate-oxide reliability. Structure stress created in SWAMI is smaller than in PBL and LOCOS. Maximum stress XY created in LOCOS is greater than in SWAMI, but less than PBL.

Integration degree of IC is important in electronics technologies. Using thermal oxidation micro scale into nano scale conversion aren’t the same as reduce structures dimensions and technological parameters N times if integration degree of IC is N. What happens if we reduce all dimensions and technological parameters 10 times? Results are shown in Fig. 6 – 8.

**Fig. 6.** Stress XY in Local Oxidation of Silicon in nano scale (t=12 min., T=1000 ºC, SiO2=2 nm, Si3N4=15 nm, σ\(_{xy\text{ max}}\) = 1,44·10\(^{11}\) dyne/cm\(^2\), σ\(_{xy\text{ struct}}\) = -7,09·10\(^9\) dyne/cm\(^2\))

**Fig. 7.** Stress XY in Poly-Buffered Local Oxidation of Silicon in nano scale (t=12 min., T=1000 ºC, SiO2=2 nm, poly Si=10 nm, Si3N4=15 nm, σ\(_{xy\text{ max}}\) = 2,09·10\(^{11}\) dyne/cm\(^2\), σ\(_{xy\text{ struct}}\) = -7,09·10\(^9\) dyne/cm\(^2\))

In LOCOS structure grown silicon oxide doesn’t have isolation oxide form with attributes, gate zone is modified. The main plus is that silicon nitride is without of stress and defects (compare Fig. 3 and Fig. 6). Stress XY value is σ\(_{xy\text{ max}}\) = 1,44·10\(^{11}\) dyne/cm\(^2\), σ\(_{xy\text{ struct}}\) = -7,09·10\(^9\) dyne/cm\(^2\). Grown silicon oxide has more stress and defects.
(compare Fig. 4 and Fig. 7) and in this structure polysilicon has gone in deep gate zone during thermal oxidation in PBL structure ($\sigma_{xy, max} = 2.09\cdot10^{11}$ dyne/cm$^2$, $\sigma_{xy, struct} = 2.79\cdot10^{10}$ dyne/cm$^2$).

As mentioned above polysilicon removal can cause severe gate-oxide reliability problems. The best results are achieved with SWAMI technology, where best form and less stress ($\sigma_{xy, max} = 7.26\cdot10^{10}$ dyne/cm$^2$, $\sigma_{xy, struct} = 4.59\cdot10^{10}$ dyne/cm$^2$) and defects appear according to micro scale structure. In this case silicon nitride is modified a little and stress in silicon oxide appeared only in one line (Fig. 8). Structure stress created in SWAMI is smaller than in PBL and LOCOS. Maximum stress XY created in LOCOS is greater than in SWAMI, but less than PBL in nano scale structures.

When compared different structures in scale level, in nano scale all structures have greater stress than in micro scale.

Fig. 8. Stress XY in Side Wall Masked Isolation in nano scale ($t_1=0.4\text{ min.}, t_2=50\text{ min.}, T=1000\text{ ºC}, \text{SiO}_2=4\text{ nm, Si}_3\text{N}_4 =16\text{ nm, Si}_3\text{N}_4 (2\text{th})=4\text{ nm, }\sigma_{xy, max} = 7.26\cdot10^{10}$ dyne/cm$^2$, $\sigma_{xy, struct} = 4.59\cdot10^{10}$ dyne/cm$^2$).

Conclusions

1. Stress depends on technologies type (LOCOS, PBL, SWAMI) in thermal oxidation.


Problems of thermal oxidation, related with LOCOS, PBL and SWAMI technologies were researched. The stresses, which appear during thermal oxidation are analysed in micro and nano scales levels in mentioned technologies. Thermal oxidation process is simulated with ATHENA. The Deal-Grove model is used for the oxide growth kinetics. Both in micro and nano scale structures stress created in SWAMI is less than in PBL and LOCOS. Maximum stress created in LOCOS is greater than in SWAMI, but less than PBL. Using thermal oxidation in nano scale created stresses are greater than in micro scale structures. Ill. 8, bibl. 7 (in English; summaries in English, Russian and Lithuanian).

References


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