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Modelling and Fabrication of Micro-SOFC Membrane Structure

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Fabrication process of micro-SOFC membrane structure using the bulk micromachining of silicon technique with SiO_2 and Si_3N_4 sacrificial layers is presented in this study. The process involves back side photolithography, magnetron sputtering of platinum thin films, thermal evaporation of YSZ electrolyte, deep reactive ion etching of silicon, and, finally, release of free-standing membrane using CF_4/O_2 plasma etching. X-ray analysis shows the cubic phase of YSZ electrolyte and platinum electrodes. Modelling of normal stress distribution in the micro-SOFC structure with the Si_3N_4 sacrificial layer shows that at high temperatures the substrate expands less than the coating, causing tensile stresses in the substrate area next to the coating and compressive stresses in the coating, as the substrate material has a lower coefficient of thermal expansion than the layered Pt/YSZ/Pt coating.

Keywords: micro-solid oxide fuel cell, bulk micromachining, Pt/YSZ/Pt membrane, stress modelling.

1. INTRODUCTION

Micro-solid oxide fuel cells (micro-SOFC) due to their high efficiency and energy density seem to be very attractive electrochemical power source for mobile devices. Micro-SOFC can be fabricated using conventional thin film deposition and patterning techniques and many types of fuel cells varying in their geometry and employed materials have been developed up to this time. Review article [1] describes achievements of different scientific groups developing the micro-SOFC. It was shown that mechanical and thermal stability as well as reliability of micro-SOFC is largely determined by the size of membrane and materials properties, so it is very important to choose the right device technology route, geometry and materials of thin film electrode and sacrificial layer. Thickness of the electrode membrane in different works varies from the parts up to a few micrometers, when the area of membrane varies from a few square micrometers up to the twenty millimetres [2, 3]. For example, silicon bulk micromachining was successfully applied [4] to fabricate thin film membrane structure (thickness of membrane 220 nm, active area size varied from 20 to 100 square micrometers). 300 nm thick thin film membrane (active area size varied from 50 to 240 square micrometers) was fabricated using sputtering, lithography, and deep etching [5]. In other work a corrugated micro-SOFC membrane was fabricated on the prepatterned silicon substrate in order to increase the active surface area and mechanical strength of membrane as well as resistance to the thermal stress of the layered membrane structure [6]. Two-step fabrication technique of SiO_2/Si membrane combining the deep wet silicon etching and SF_6/O_2 reactive ion etching was demonstrated in [7]. Here, simulation revealed that increase in size of the membrane contributes to the rise of deformations as well as stresses at the membrane edges and corners. Very recent development [8] describes fabrication of composite SiO_2/Si_3N_4 membrane obtained using wet silicon etching in KOH solution following removal of SiO_2 layer in order to obtain Si_3N_4 membrane (thickness of Si_3N_4 membrane 300 nm, active area size varied from 50 to 820 square micrometers). Other recent development [9] also utilizes Si_3N_4 insulating layer to deposit 75 nm – 150 nm thick yttria-stabilized zirconia (YSZ) electrolyte, a 40 nm – 80 nm porous Pt anode, and a 130 nm porous Pt cathode. Recently, it was shown, that Pt anode can be successfully replaced [10] by nanoporous palladium (Pd) film or ruthenium and gadolinia-doped ceria composite nano-crystalline thin film [11]. Thickness effects of yttria doped ceria interlayers on solid oxide fuel cells [12] and mechanical and thermal stability of free standing membranes was studied in [13, 14]. Modelling shows [14] that edge clamped thin film membrane presents multi-stage wrinkles (the largest ones are in the center and the smaller ones near the clamped boundary) and the largest tensile stress is close to the clamped boundary. The aim of our work is modelling of micro-SOFC membrane structure in a large temperature range and finally fabrication of Pt/YSZ/Pt thin film triplex using Si_3N_4 or SiO_2 sacrificial layers.

2. MODELLING

Micro-SOFC is very delicate and fragile structure, consisting of several thin layers, whose working temperature can reach up to 800 ºC. Mechanical properties of a device working under such severe environmental conditions have to be examined very closely in order to improve reliability and prevent failures. One of the most evident causes for failure is thermal stress. Thermal stress arises due to difference in coefficients of thermal expansion of interfacing layers. When the stress is too large it can cause various failures e. g. cracking of a layer

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is possible when tensile stress develops, while delamination can occur if stress is compressive [15].

In our model we analyze thermal stress in a layered Pt/YSZ/Pt micro-SOFC structure on the Si substrate with Si_3N_4 (200 nm thick) and SiO_2 (200 nm thick) sacrificial layers, respectively. We aim to map stress distribution in a whole structure in the range of working temperatures (200 ºC – 800 ºC) and to determine, which of the sacrificial layers is more beneficial for the thermal stability. This model contains only thermal loads, which are calculated according to the following equations:

$$\sigma = D\varepsilon_{el} + \sigma_0 = D(\varepsilon - \varepsilon_{th} - \varepsilon_0) + \sigma_0 \quad (1)$$

and

$$\varepsilon_{th} = \begin{bmatrix} \varepsilon_x \\ \varepsilon_y \\ \varepsilon_z \\ y_{xy} \\ y_{yz} \\ y_{xz} \end{bmatrix} = \alpha(T - T_0), \quad (2)$$

where σ is the stress vector, D is the elasticity matrix, ε_x, ε_y, ε_z, γ_{xy}, γ_{yz}, γ_{xz} are the strain components, α is the coefficient of thermal expansion, T is the actual temperature, and T_0 is the reference temperature.

Simulation was done using "Comsol Solid Mechanics" module. Two-dimensional geometry was used to represent cross-section of the micro-SOFC structure. The upper-left corner of the structure is fixed, and the upper-right corner is constrained in the y direction (Fig. 1). This prevents rigid-body movements but does not affect the stress distribution. It was assumed that z component of the strain is zero. In the model we have considered that the sacrificial layers of Si_3N_4 and SiO_2 were commercially made on the Si substrate. The platinum electrodes (200 nm thick) and YSZ layer (400 nm thick) were deposited at 20 ºC and 200 ºC, respectively. We assumed that at the time of layer deposition, depositing layer is stress-free and all former layers have residual stress resulting from the previous processes. This is not entirely true in a real world because there also is an intrinsic stress that arises during deposition process due to mismatch of the lattice constants between different layers, grain growth, defect annihilation, etc. [15]. The mechanisms generating intrinsic stresses are not well characterized quantitatively, so in this model they are not considered. Finally thermal stability of the whole SOFC structure was tested in the range of working temperatures.

Fig. 1, a, shows the normal stress (x component) distribution in the micro-SOFC structure with the Si_3N_4 sacrificial layer. The silicon substrate has a lower coefficient of thermal expansion than the layered Pt/YSZ/Pt coating. This means that the substrate expands less than the coating, causing tensile stresses in the substrate area next to the coating and compressive stresses in the coating.

Fig. 1, b, shows the normal stress distribution (x component) in the micro-SOFC structure with the SiO_2 sacrificial layer. Compared with previous case the thermal stress distribution pattern is very similar. Compressive stress value in YSZ layer is almost the same in both cases. Although tensile stress in the SiO_2 sacrificial layer and substrate is much smaller as compared with the previous case whereas a sacrificial layer Si_3N_4 was used. It should be noted that in the first case (Fig. 1, a) most of the tensile stress is located in Si_3N_4 layer, in the second case (Fig. 1, b) it is more penetrated into substrate and more evenly distributed between the sacrificial and substrate layers.

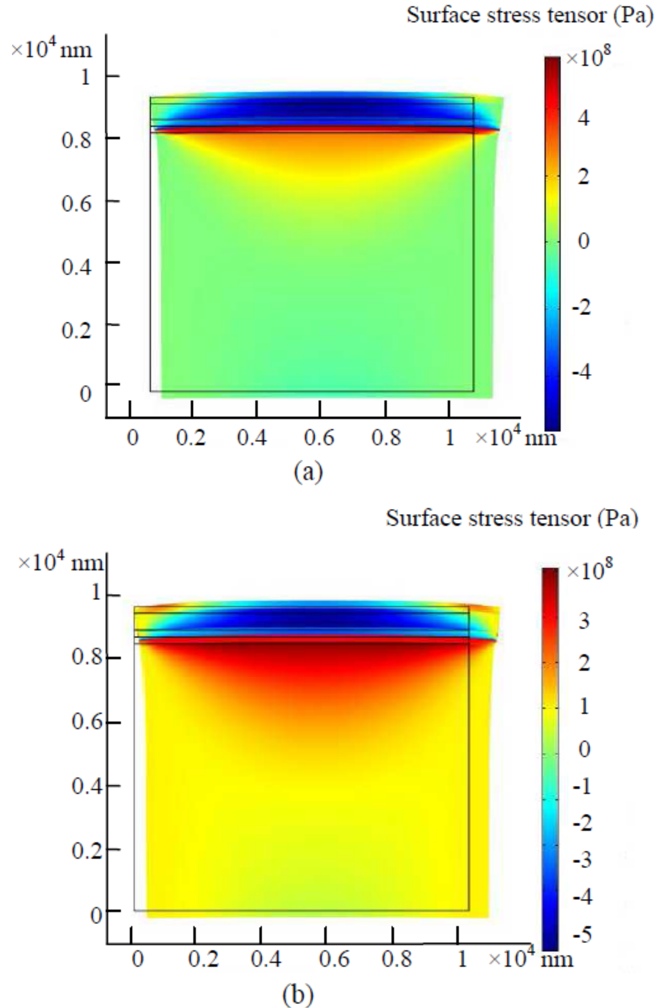

Fig. 1. Thermal stress in micro-SOFC structure: a – with Si_3N_4 sacrificial layer at 600 ºC temperature; b – with SiO_2 sacrificial layer at 600 ºC temperature

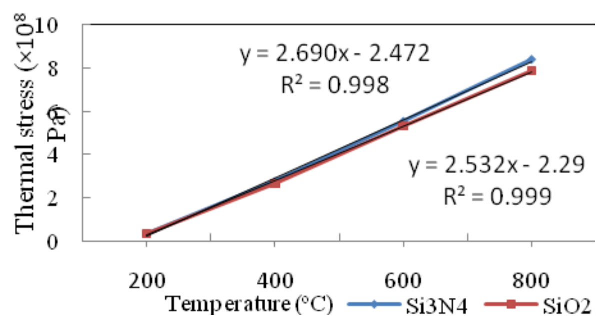

Fig. 2. Thermal stress dependence on temperature in YSZ layer of micro-SOFC structure with Si_3N_4 and SiO_2 sacrificial layers

Fig. 2 shows the normal stress in (x component) dependence on temperature in the YSZ layer in the

micro-SOFC structure with the Si_3N_4 and SiO_2 sacrificial layers. Thermal stress distribution retains the linear approximation. The difference in thermal stress developed in YSZ layer, compared between Si_3N_4 and SiO_2 sacrificial layers, is negligible.

In the similar fashion thermal stress distribution in micro-SOFC membrane structure was also investigated. Width of the simulated membrane is 100 µm. Fig. 3 shows the normal stress (x component) distribution in the micro-SOFC membrane structure with the Si_3N_4 sacrificial layer. The layered Pt/YSZ/Pt coating, which is sitting on silicon substrate, is experiencing quite substantial compressive stress due to differences in coefficients of thermal expansion in between substrate and the layered Pt/YSZ/Pt coating. Stress distribution pattern is very similar to one presented in Fig. 1, a, case. At the same time in membrane, which is not restricted by substrate accumulated compressive thermal stress is significantly lover, because membrane has a room to expand. This kind of expansion causes deformation of the membrane. Fig. 4 shows thermal stress distribution in the YSZ layer across the structure. As one can see stress decreases significantly in the membrane area (100 µm – 200 µm coordinate).

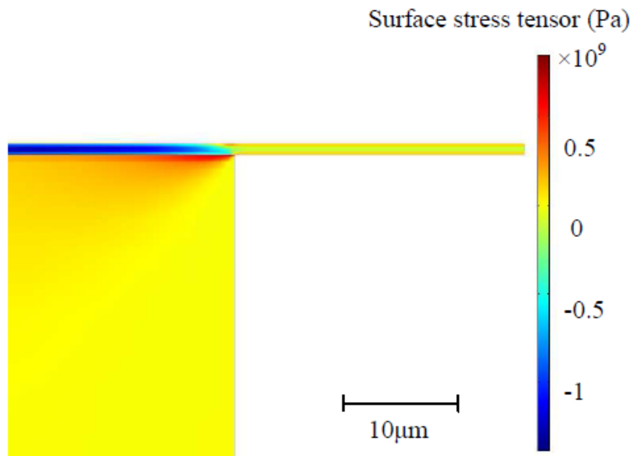

Fig. 3. Thermal stress distribution map of micro-SOFC membrane (Si_3N_4 sacrificial layer) at 800 ºC temperature

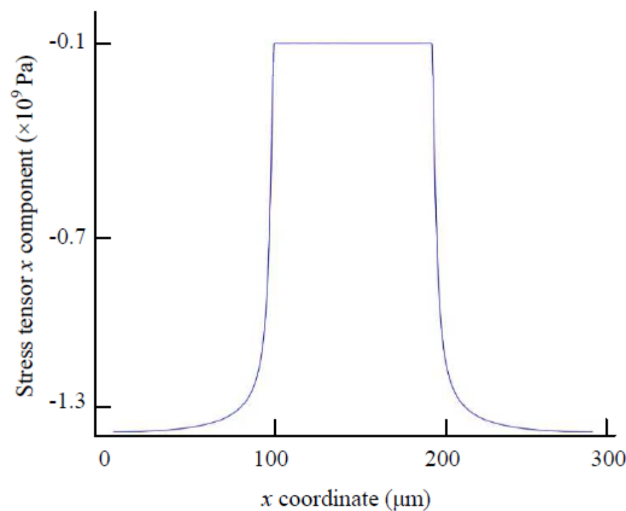

Fig. 4. Thermal stress distribution in YSZ layer of micro-SOFC membrane (Si_3N_4 sacrificial layer) at 800 ºC temperature

3. EXPERIMENTAL TECHNIQUES AND RESULTS

According the modelling results the corresponding geometry was chosen and the fabrication process of micro-SOFC free-standing membrane is shown in Fig. 3. Low pressure chemical vapour deposition (LPCVD) was used to grow the 500 nm thick layer of low-stress Si_3N_4 (or SiO_2 1 µm thick) on both sides of double side polished single crystal Si (100) wafer of 100 mm diameter. Back side photolithography was carried out in order to define pre-membrane opening windows following CF_4/O_2 plasma etching of silicon nitride.

Pt thin film with thickness of 200 nm (positive electrode) was deposited by direct current (DC) magnetron sputtering source ("Kurt J. Lesker" company), which was integrated in a "Leybold Heraeus-A-700-QE" device vacuum system. A turbomolecular pump was used to evacuate the main chamber to a base pressure of 2×10^{-4} Pa. The sputtering gas was argon of 99.996 % purity, and pressure in the chamber was 7×10^{-1} Pa. The Pt target (purity 99.99 %) with a diameter of 2 inch was located at a target-substrate distance of 16 cm and exhibited a tilt angle of 30 degrees with respect to the substrate position. The substrate holder was rotated during the deposition process in order to obtain homogeneous distribution of the film thickness. Thin film deposition process was carried out at room temperature. The magnetron voltage was 510 V, and current was 0.4 A. The growth rate was determined by a quartz sensor. These sputtering conditions yielded a deposition rate of 0.28 nm/s. After deposition of positive electrode mask alignment and photoresist patterning on top surface was carried out in order to define membrane area. In order to obtain the disks used as the source material for e-beam evaporation of electrolyte, the commercial yttria stabilized zirconia (8YSZ from "Tosoh") ceramic powders containing 8 mol % of Y_2O_3 were pressed into pellets of 10 mm in diameter. Thin film of 8YSZ was evaporated on the photoresist pre-patterned substrate. Evaporation was performed at a pressure of 7×10^{-1} Pa, and the e-gun power was 10 kW. During the evaporation process, a temperature of the substrate was kept constant at around 200 °C and the thickness of the thin film was controlled by the quartz sensor. Evaporation rate of 8YSZ was 0.6 nm/s.

Pt thin film cathode (negative electrode) was sputtered at the same conditions, as positive electrode. The thickness of negative electrode was 200 nm (defined from SEM analysis Fig. 4). Lift-off technique was used to remove selectively YSZ and cathode thin films dissolving resist away in a solvent. The deep reactive ion etching (DRIE) of silicon was done using the STS ICP system (Surface Technology Systems). Bosch process, also known as pulsed etching, which alternates between etching and polymerization modes to get vertical etch walls, was used to etch silicon through the wafer up to the silicon nitride film (Fig. 5).

DRIE conditions are defined by many parameters such as gas-flow rate, RF power, inductive couple plasma (ICP) source power, chamber pressure and stage (bottom electrode) temperature that affect the etch rate, profile and uniformity of etch patterns throughout the sample. Bosch process parameters are providing high aspect ratio of DRIE (Fig. 7) in Table 1.

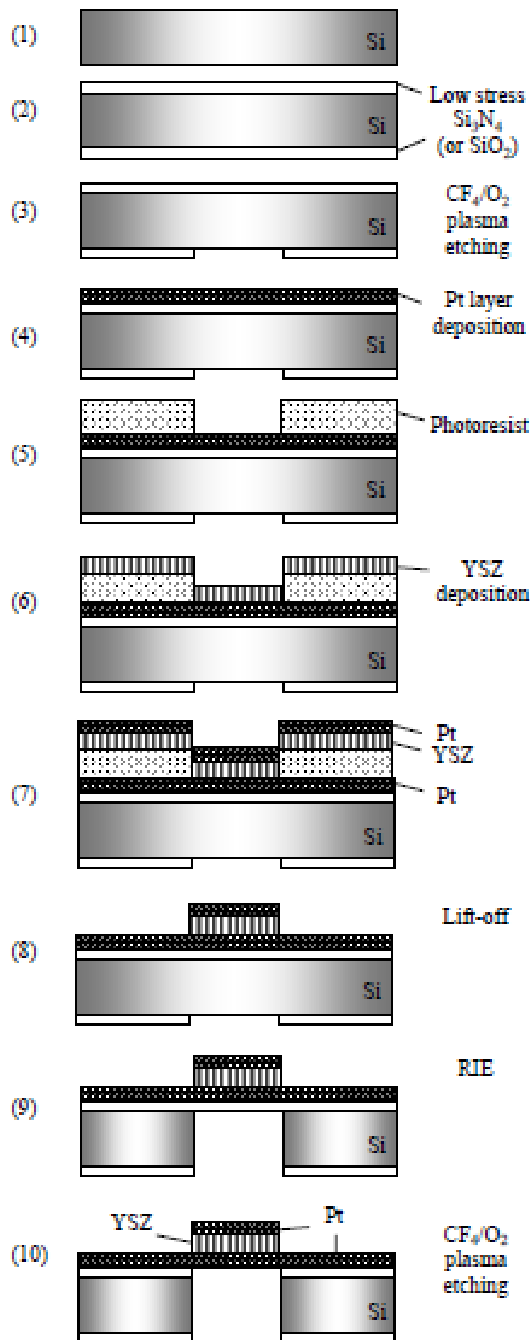

Fig. 5. Fabrication process of micro solid oxide fuel cell free-standing membrane: 1 – double side polished single crystal Si <100> substrate; 2 – chemical vapour deposition (LPCVD) of low-stress Si_3N_4; 3 – back side photolithography and silicon nitride CF_4/O_2 plasma etching; 4 – dc magnetron sputtering of platinum thin film anode; 5 – mask alignment and photoresist patterning on top surface; 6 – e-beam deposition of YSZ thin layer; 7 – dc magnetron sputtering of platinum thin film cathode; 8 – lift-off of YSZ and cathode thin films; 9 – high aspect ratio deep reactive ion etching (RIE); 10 – silicon nitride CF_4/O_2 plasma etching and release of free-standing membrane

Prior to the Bosch process, auxiliary 300 nm-thick Al layer was evaporated and patterned on a back surface, as pure silicon nitride layer can be attacked by the process gas plasma. After Bosch process, the auxiliary Al layer was removed using the Al etchant (Al-12S, "Sunchem AB"). Finally, silicon nitride film in the membrane area was removed away using CF_4/O_2 gas plasma and free-standing membrane was released.

Table 1. Deep reactive ion etching (Bosch process) conditions

Parameter	Passivation phase	Etch phase
Cycle time (s)	7	10
Pressure (Pa)	2.4	4.7
C_4F_8 gas flow (sccm)	80	0
SF_6 gas flow (sccm)	0	130
O_2 gas flow (sccm)	0	13
ICP source power (W)	600	600
Bias power (W)	0	20
Bottom electrode chiller temperature (ºC)	15	15
Etch rate (μm/min)	3.5	

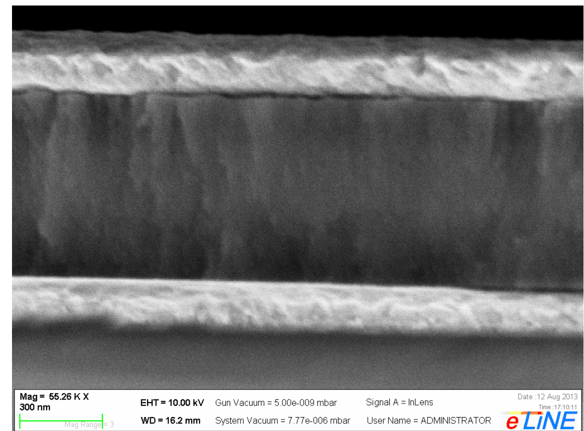

Fig. 6.SEM photograph of Pt/YSZ/Pt membrane structure

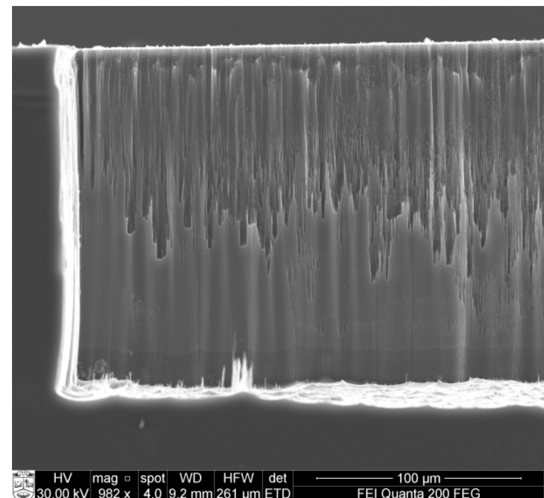

Fig. 7. SEM photograph illustrates high aspect ratio deep reactive ion etching (Bosch process)

Structure and crystallographic orientations of micro-SOFC membrane structure ($Si/SiO_2/Pt/YSZ/Pt$) were identified by X-ray diffraction analysis (XRD) using $CuK_α$ radiation on a Bruker AXS GmbH diffractometer with standard Bragg-Brentano focusing geometry. The peak intensities were measured in the 20°–90° $2θ$ range with a

step size of 0.01° and a counting rate of 2 s per scanning step.

XRD pattern Pt/YSZ/Pt on Si substrate with SiO_2 sacrificial layer membrane structure is displayed in Fig. 8. The peak positions of the (111), (200), (220), (311) and (222) reflections correspond to the typical crystal structure of the magnetron sputtered platinum film [16]. In the scan range ($25° \leq 2\theta \leq 90°$) (101), (110), (220) and (211) reflections of electron beam evaporated YSZ were established. It can be assumed, that platinum electrodes and YSZ electrolyte have cubic crystalline structure with typical columnar growth and grains size.

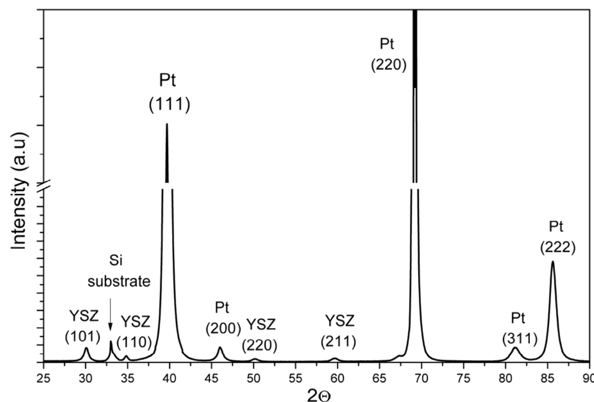

Fig. 8. XRD pattern of Pt/YSZ/Pt on Si substrate with SiO_2 sacrificial layer structure

4. CONCLUSIONS

1. Silicon bulk micromachining technique with Si_3N_4 and SiO_2 sacrificial layers was used to produce Pt/YSZ/Pt membrane for micro-SOFC and thermal stress was analyzed using "Comsol Solid Mechanics" module.

2. Stress analysis in the micro-SOFC membrane structure with the Si_3N_4 sacrificial layer shows that the substrate expands less than the coating, causing tensile stresses in the substrate next to the coating boundary and compressive stresses in the coating itself. Normal stress dependence on temperature in the YSZ layer is linear, and absolute value changes from 6.81×10^7 Pa at 200 °C to 8.49×10^8 Pa at 800 °C.

3. XRD results show that Pt/YSZ/Pt membrane structure has crystallite orientations specific to the composite texture of electrolyte thin film.

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