Operating point of Capacitive Micromachined Ultrasonic Transducers with Sub-structural Elements

I. Morkvenaite-Vilkonciene¹, D. Virzonis², G. Vanagas², V. Krikscikas³ ¹Department of Electricity and Electronics, Panevezys College, Laisves av. 23, Panevezys, phone: +370 683 61345 ²Department of Electrical Engineering, Kaunas University of Technology Panevezys Institute, Klaipedos St. 3, Panevezys, phones: +370 687 13551, +370 620 20460 ³UAB Minatech, Pilenu St. 30, Panevezys, phone: +370 682 62458 inga.vilkonciene@panko.lt

Abstract—CMUT FEM 2D electrostatic model was created to investigate dielectric surface roughness influence to the operating point. Three different form structures: triangle, halfcircle, rectangle were investigated. The highest electric field norm concentration on the triangle apex was found. For experiments, dielectric surface was etched by two etching steps to define the cavity: reactive ion etching and buffered oxide etching for smoothing the cavity bottom. Atomic force microscopy was used to monitor and control the roughness of the cavity bottom. The simulation showed the decrease of the effective gap by 0.6 % and 1.0 % in 10 and 20 nm RMS cases, respectively. Voltage-capacitance tests of the fabricated devices with known roughness values confirmed the assumptions about the roughness-induced operating point shifts.

Index Terms—Etching, ultrasonic transducers, surface roughness, finite element methods.

I. INTRODUCTION

One of the important aspects of CMUT (capacitive micromachined ultrasound transducers) technology is the technology-determined control over the operating voltage. Particularly, the uncertainty and scatter of the effective gap between the electrodes is undesirable since highly non-linear relationship between the collapse (pull-in) voltage and the effective gap always exists [1]. On the other hand, for device sensitivity and maximum value of electromechanical transfer coefficient, bias voltage has to be close to the collapse voltage, and practical value of $V_{bias}=0.8V_{collapse}$ is often chosen for operating point. The uncertainty and scatter of the cell gap height is more specific for the surface micromachining approach, especially if in-cavity deposition is used [2]. The same reference shows that surface roughness of the cavity bottom has the influence on the CMUT operating point, because it changes the actual cavity height.

Manuscript received March 11, 2012; accepted May 22, 2012.

In this work we examined the discarded distribution of the electrical field in a cavity as a result of the dielectric layer roughness and corresponding operating point shift. This research was also designated to test the proprietary CMUT fabrication technology [3], [4].

II. THEORY AND ANALYSIS METHODS USED

CMUT operating point can be found from the lumped element model subjected to electrostatic and spring force equilibrium, which can be stable and unstable. Stable values are when the CMUT cell membrane is deflected for less than $g_0/3$. Here g_0 is the effective gap between the electrodes at rest position with zero voltage. If the membrane is deflected for more than $g_0/3$ by the voltage applied, the pull-in (collapse) phenomenon occurs [5]. The approximate value of the collapse voltage can be found by the following equation

$$V_{coll} = \sqrt{\frac{8kg_0^3}{27\epsilon A}},\tag{1}$$

where k stands for equivalent spring stiffness coefficient, ε stands for effective dielectric permittivity of the gap between the electrodes, *A* is the effective area of the electrodes.

The effective dielectric permittivity can be found if the capacitance and the gap are known [5]

$$\varepsilon = \frac{C \cdot g_0}{A},\tag{2}$$

where *C* is capacitance, and g_0 is the actual gap. Substituting the equations (1) and (2) we have

$$V_{coll} = \sqrt{\frac{8kg_0^2}{27C}}.$$
 (3)

The effective capacitance of the CMUT cell can be found

This research was funded by a grant (No. MIP-059/2012) from the Research Council of Lithuania. It was performed in collaboration with UAB Minatech.

from the relationship between the capacitance and stored energy

$$C = \frac{2 \cdot W(g_0)}{V^2}.$$
(4)

We also can express the gap as a function of the stored energy and applied voltage

$$g_0 = \varepsilon \frac{A \cdot V^2}{2 \cdot W(g_0)}.$$
 (5)

The sub-structural elements on the cavity bottom introduce the change of the electrical energy $\Delta W(g)$, which can be expressed as the change of the effective gap Δg

$$g_0 - \Delta g = \varepsilon \frac{A \cdot V^2}{2 \cdot (W(g_0) + \Delta W(g_0))}.$$
 (6)

We created 2D finite element analysis (FEA) model of the gap of the CMUT cell to find the accumulated energy $W(g_0)$ with applied bias voltage *V* and with simulated roughness of the bottom dielectric layer. Then the actual collapse voltage was found from the equation (3) with effective gap change (6).

The roughness of the dielectric layer was mimicked by introducing the features with half-circle, rectangular and triangular cross-sections. In all three cases the cross-section area was kept constant. The actual dimensions of the simulated features was chosen to mimic the statistical roughness values of 10 nm and 20 nm RMS. Another limitation for simulated roughness was to keep the average vacuum gap equal to g value (Fig. 1), which corresponds to the designed vacuum gap. The structure of the model is shown at the Fig. 1, illustrating smooth dielectric surface (a) and the rough surface (b) with only triangular cross-section features displayed. The voltage is applied over the "electrical gap" (g₀, Fig 1.) between the upper aluminum electrode and the bottom silicon electrode which is supposed to be highly conductive. Model parameters are shown in the Table I.

To describe the operating point of CMUT we used the spring and Coulomb forces as the functions of the gap. The Coulomb force was found using following equation

$$F_C = \frac{W(g)}{g} \tag{7}$$

and the spring force, correspondingly

$$F_s = k \cdot \Delta g. \tag{8}$$

Roughness measurements of the CMUT cavity bottom was done with AFM (atomic force microscope), working in contact mode. We used the monocrystal silicon cantilever CONTR with the tip radius less than 8 nm. Cantilever dimensions: width, thickness and length: 50 μ m, 2 μ m, 450 μ m. AFM scanning process was performed at 5.5 μ m/s speed.

The voltage-capacitance relationship of the fabricated devices was measured using the probing station, direct current voltage supply and the capacity meter.

III. ELECTRIC FIELD SIMULATION



Fig. 1. Finite element 2D model of a CMUT cell gap with smooth dielectric surface (a) and SiO_2 substructures (b), which mimic the dielectric film roughness.

TABLE I. PARAMETERS OF FEA MODEL.								
Parameter		Dimension			Material			
Membrane radius		20 µm			DECVD			
Membrane thickness			0.5 μm			PEC VD		
Membrane stiffness coefficient			5307 N/m			mulue		
Top electrode thickness			0.4 μm			Al		
Vacuum gap			0.15 µm			-		
Isolating layer thickness		().02 μm		SiO ₂			
Materials properties	Si		SiO ₂	Al		Si_3N_4		
Density, kg/m3	2330		2200	2700		3100		
Relative permittivity	11.7		3.7	8		5.4		
Elasticity modulus, GPa	150		70	70		320		
Poisson's ratio	0.17		0.17	0.35		0.23		
Electrical conductivity, S/µm	0		0	35.5		0		

Simulated electric field norm distribution over the CMUT gap with the roughness features of different cross- section is shown on the Fig. 2. It can be observed that intensity of the electric field norm exhibits the large peaks at the top of the features and even distribution over the rest of the vacuum gap. The electric field norm is close to zero within the bottom electrode (less or equal to 0 height) and membrane at 150 nm or larger height value. Profiles of electrical field norm distributions (shown in Fig. 3) for all three roughness types were obtained at the symmetry axis of each feature.

From these profiles we conclude that features of triangular cross-section maximally distort the electrical field, because the electric field norm peak is highest in the triangular cross-section case (Fig. 3). Therefore we further simulated only "triangular" roughness type.

Triangle sectioned structures of ± 5 nm and ± 10 nm from the nominal g value were simulated to get roughness values of 10 nm and 20 nm RMS, respectively.

Fig. 4 illustrates the CMUT operating point in terms of Coulomb and equivalent spring forces as gap height change functions. Membrane equilibrium position can be found at the intersection of corresponding lines. The illustrated case is for 14.4 V bias, when the nominal (zero roughness) collapse voltage is 24 V. So, it describes $0.6 V_{collapse}$ operating point. The unstable equilibrium points of Coulomb and spring forces at the right part of the graph illustrate how the actual operating point will be affected by the roughness-distorted electrical field. The effect of the distorted electric field was evaluated as the 0.6% and 1.0% change of the

effective gap using the equation (6).



Fig. 2. Electric field norm of different form SiO_2 structures with the same area on the SiO_2 cavity bottom.



Fig. 3. Electric field distribution in three different structures with the same area.



Fig. 4. Electrostatic and spring force dependence on gap change with 14.4 V bias voltage.

IV. FABRICATION OF CMUTS AND ROUGHNESS MEASUREMENTS

Highly doped silicon <100> substrate with 0.5 µm thermal oxide layer was used for CMUT micromachining. Schematic representation of the technological sequence is shown in the Fig. 5. Cavity bottom roughness measurements

were taken after definition and etching of the cavities in step b). The etching process was made in two steps: 1) anisotropic CF4 reactive ion etching (RIE) and 2) isotropic buffered oxide etch (BOE) step for smoothing down the cavity bottom. RIE parameters: time: 5 min, 40 sccm/min CF4, power of plasma: 250 W, pressure: 100 mPa. BOE concentration: 40% NH3F:HF 6:1, etching time from 0 to 60 s; roughness measurements were taken every 10 s.



Fig. 5. Schematical representation of technological process used for CMUT fabrication: a) – silicon wafer with 0.5 μ m thermal oxide; b) – cavity definition and etching down to the oxide; c) – sacrificial film deposition; d) – first structural nitride deposition; e) – sacrificial etching trough the vials; f) – second structural nitride deposition and sealing of the cavities; g) – top electrodes deposition and patterning.

It can be seen from the Fig. 6 that the cavity bottom has considerably increased roughness (12.3 RMS) after the RIE step and it is smoothed down by the BOE step with



Fig. 6. Roughness root mean square values dependence on BOE time.

minimum achieved roughness of 2.5 nm RMS after 30 s etch. Further increase of the BOE step time was found to be related with slight increase of the roughness to the 3.2 nm RMS. The error bars represent the scatter from the mean value of 3 - 5 samples at each point.

V. TESTS OF CMUTS WITH DIFFERENT CAVITY ROUGHNESS

We measured the voltage-capacitance relationships for two CMUT devices with known initial (from AFM inspection after step b, Fig. 6) roughness values to compare their performance. The dimensions of the CMUT cells are the same as the simulation data presented in Table 1. The 180 cells were connected in parallel to form the elements, and measurements were carried on the single element. The overall view of the fabricated cells is shown on the Fig 7.



Fig. 7. Optical profilometer image shows the fragment of the fabricated CMUT.

Fig. 8 shows measured voltage-capacitance (C/V) relationships of two devices with different roughness of the cavity bottom. The collapse voltage can be determined from the voltage-capacitance relationship as the breakpoint, where the C/V ratio changes. This corresponds to the situation, when the gap cannot decrease further. The measured collapse voltages are 32 V for the device with 12.3 nm RMS and 35 V for the device with 2.5 nm RMS cavity roughness. The experimental data were fitted with the simulated curves for different effective gap values, which are 138 nm and 153 nm correspondingly. The drop of the measured capacitance value after the collapse we relate with increased injection of the charged particles to the insulating film.

The 10 nm gap difference can be explained by the mechanical gap decrease due the increased roughness (12.3 nm vs 2.5 nm), and the discarded electrical field is responsible for the rest 5 nm difference (total effective gap difference is 15 nm, as we see from the fitted results). This is 3.3 % from the design value of 150 nm, which is quite close to the proportion found during the electrical field distribution simulation.



Fig. 8. Measured voltage/capacitance relationships of two devices with 2.5 nm and 12.3 nm roughness of the cavity and the same designed gap value, model-fitted for 138 nm and 153 nm gap.

VI. CONCLUSIONS

We have found that cavity bottom roughness is distorting the electrical field distribution and can cause the shift the CMUT operating point even if the average gap height remains equal to the designed gap height. As shown by simulation, triangle roughness structures on the dielectric surface can cause the effective gap deviation 0.6% and 1.0 % in 10 nm and 20 nm RMS cases, respectively. This assumption was confirmed experimentally by showing that CMUTs with increased cavity bottom roughness have lower collapse voltage and larger device capacitance, which cannot be fully explained by the mechanical gap decrease. Therefore we attribute the 3.3 % effective gap change to the distorted electrical field.

REFERENCES

- I. O. Wygant, M. Kupnik, B. T. Khuri-Yakub, "Analytically calculating membrane displacement and the equivalent circuit model of a circular CMUT cell", in *Proc. of the IEEE Ultrasonics Symposium*, 2008, pp. 2111–2114.
- [2] L. Der-Song, "6F-5 Characterization of Fabrication Related Gap-Height Variations in Capacitive Micromachined Ultrasonic Transducers", in *Proc. of the IEEE Ultrasonics Symposium*, 2007, pp. 523–526.
- [3] D. Virzonis, et al., "Capacitive micromachined ultrasonic transducer and its fabrication method", European patent application, 2010, p. 12.
- [4] G. Vanagas, D. Viržonis, V. Paukštaitis, D. Baranauskas, S. Červiakov, "Integrated Front End Electronics Design for Micromachined Ultrasound Transducers", *Elektronika ir Elektrotechnika (Electronics and Electrical Engineering)*, no. 7, pp. 117–120, 2010.
- [5] S. D. Senturia, *Microsystem Design*. Kluwer Academic Publishers, 2002, p. 689.