ELECTRONICS AND ELECTRICAL ENGINEERING
ISSN 1392 – 1215 2010. No. 10(106)
ELEKTRONIKA IR ELEKTROTECHNIKA

T 171 MICROELECTRONICS
MIKROELEKTRONIKA

Simulation of the MOS Transistors Structures Channel Technological Problems

V. Kašauskas, R. Anilionis, D. Eidukas
Department of Electronics Engineering, Kaunas University of Technology,
Studentų str. 50, LT-51368 Kaunas, Lithuania, phone: +370 37 35 13 89, e-mails: vytautas.kasauskas@gmail.com, romualdas.anilionis@ktu.lt

Introduction

The influence of different processes to the MOS transistor output parameters is different. It is therefore important to know optimal technological parameters in the production of different manufacturing types of MOS transistors, especially if the purpose is to achieve the same channel length.

In this work, the models of technological processes for the production of different technological routes of MOS transistors are prepared. The main attention is focused on the channel formation, its structural problems using the ion implantation (II) technological process. Effects of II technological modes to the transistor output characteristics. The simulation results are presented. Athena and Atlas software are used for the simulation. Technological problems of structure of the selected types of MOS with the channel length L of less than 90 nm obtained during the simulation are analysed.

Selection and preparation of the mathematical model

In the production of MOS transistors where the L is less than 90 nm, it is important to determine the appropriate and optimal modes of technological operations. II process operations are important in ensuring the accuracy of the L, in reducing the width of the source and drain areas with the gate.

The mathematical model is done for two MOS transistor structures with different manufacturing routes. These are the MOS with the original channel length *of* L=90 nm. The cross-sectional diagram of MOS transistors with lateral impurity implantation is presented in Fig.1. [1,2]. In this particular case the gate area is first shaped, then the n^- region is formed, followed by the “spacer“ oxide and then the main source and drain areas n^+ are formed. The cross-sectional diagram of the transistor with local side "pockets" is presented in Fig. 2. [1,2]. In this case, the n^+ areas are first formed, then the gate is shaped, “spacer“ oxide, and n^- “pockets” are locally formed. In all cases, MOS transistor simulation, which is usually carried out at the design stage, is crucial to the quality parameters such as transconductance S [2].

We will use the Pearson IV function model (1) for the simulation purposes [3].

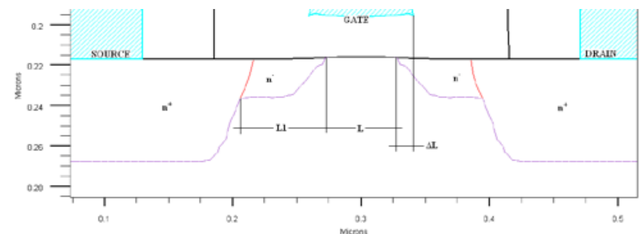

Fig. 1. Cross-sectional of the MOS transistor with lateral impurity implantation

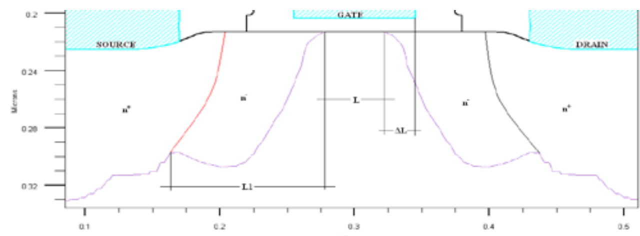

Fig. 2. Cross-sectional diagram of the MOS transistor with lateral "pocket" formation by way of ion implantation

$$\frac{df(x)}{dx} = \frac{(x-a)f(x)}{b_0 + b_1 x + b_2 x^2}, \tag{1}$$

here $f(x)$ – frequency function, a, b_0, b_1, b_2 are moments of the $f(x)$ function which are expressed in (2,3,4) equations [3]:

$$a = b_1 = -\frac{\Delta R_p \gamma(\beta + 3)}{A}, \tag{2}$$

$$b_0 = -\frac{\Delta R_p^2 \left(4\beta - 3\gamma^2\right)}{A}, \quad (3)$$

$$b_2 = -\frac{2\beta - \gamma^2 - 6}{A}, \quad (4)$$

here R_p – projected range, ΔR_p – projected range straggling or standard deviation, γ ir β – skewness and kurtosis, $A = 10\beta - 12\gamma^2 - 18$ [3].

R_p, ΔR_p, γ and β, and make four moments of the $f(x)$ function. After the evaluation of ion dose φ we can describe the distribution function of impurities according to the Pearson model (5). However, much more accurate is the Dual Pearson (DP) model in which the function of concentration of impurities can be expressed as a combination of two Pearson functions (6) [3]:

$$C(x) = \varphi f(x), \quad (5)$$

$$C(x) = \psi\left[\xi f_1(x) + (1-\xi) f_2(x)\right], \quad (6)$$

here $\psi = \varphi_1 + \varphi_2$ is the total implantation dose, and the dose variation $\xi = \varphi_1 / \psi$.

Structure of the model

Thus, the purpose of simulation is to compare the dependency of the output characteristics of the two different technological routes of MOS transistor structures with the induced channel with L<90 nm, of the main technological operations (TO) of the ion implantation n_1 and n_2. The drain and the source areas are formed with these two ion implantations. n_1 –TO with the introduction of phosphorus (P) impurities, n_2 – TO with the introduction of arsenic (As) impurities. Transistors of both technologies of NMOS type with polysilicon gate.

TO n_1 and n_2 are used in both transistors, but in different process stages. Certainly, in this case we will use the regular method and will consider other TOs of the manufacturing route as constant. Each of the ion implantation TOs depends on technological modes, the main of which are the ion dose φ and energy E. We will consider other parameters to be stable. In this way, the parameters of these two technological parameters determined for the investigation facilitate the task of determining the impact of these TOs to the channel length L and NMOS transistor output characteristics.

Each selected ion implantation TO can be described as a function of two variables $n(x,y)$, and the function of the effect of both implantations G can be expressed as (7). In this case, x is the ion implantation dose φ, and y is the energy E:

$$G = n_1(x_1, y_1) + n_2(x_2 y_2), \quad (7)$$

$$G_k = n_1(x_1, y_1) + n_2(x_2, y_2) + \ldots + n_k(x_k, y_k), \quad (8)$$

$$G_k = \sum_0^k \omega_{k-1} n_k\left(x_k, y_k\right). \quad (9)$$

We see that in the general case, the II function depends on k TO and on $k+2$ variables (8). In addition, each of the n_{k+1} of the TO II operation must be evaluated with the previous ion-implantation effect factor ω_{k-1}. Then, the expression would be (9). It should be noted that in this case the impact of other factors in the TOs production process are not assessed. Due to the number of variables and their mutual relationship it is difficult to assess the TO impact on the final electronic product, and thus on its characteristics. We see that in this case the search of optimum is very difficult.

Structural changes determined during the simulation can provide guidance to manufacturers, and predict the characteristics of the final product, in this case, the NMOS transistor output parameters.

In the NMOS transistor selected for simulation the end-ion implantations TO implant doses and energy are changing at the same mode interval. During the phosphorus implantation (for the n^- field formation) the ion dose ranges between 10^{13} cm^{-2} and 10^{14} cm^{-2}, and the energy from 1 keV to 50 keV. During the implantation of As (for the n^+ field formation) the ion dose ranges between 10^{15}cm^{-2} and 10^{16}cm^{-2}, and the energy from 1 keV to 50 keV.

Results of the simulation

In the first case the II simulation results of the NMOS transistor's n^- area formation are presented in Fig. 3. We see that during the formation of the n^- area, II technological modes must be chosen with great precision because in the entire examined II dose range, from 1x10^{13} cm^{-2} to 1x10^{14} cm^{-2}, the active induced channel length L remains limited at 5 keV and at 10 keV. If the II dose does not exceed 2x10^{13} cm^{-2}, L is observed also at 15 keV of energy. Thus, we observed the impurities underrunning the gate area, Fig. 4. However, the overlap ΔL is growing proportionally when the II energy is increased. Thus we see that during the formation of "pockets" in case of the first implantation, the orthogonal component of ion penetration R_0 is increasing, and therefore already at 2x10^{13} cm^{-2} above 40 keV we obtain the convergence of the n^- areas in the bottom section of the "pockets".

The As II is used in the formation of the main drain and source areas in the n^+. Simulation results are presented in Fig. 5. We see that in the entire selected As II dose range the channel length does not change as long as the energy does not exceed 40 keV. Upon exceeding 40 keV, the channel L is destroyed. In this case we see the impurities underrunning the gate area, as shown in Fig. 5. At high doses of As II at peak energy values we observe that the impurities underrunning under the gate area is very significant and in this case reaches 28 nm.

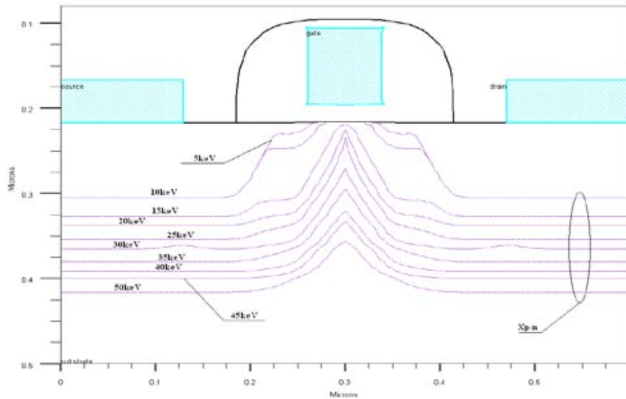

Fig. 3. Changes in structure of the NMOS transistor with lateral implantation of impurities depends on the energy for the implantation of P ions when the dose is 1x10^{14} cm^{-2}

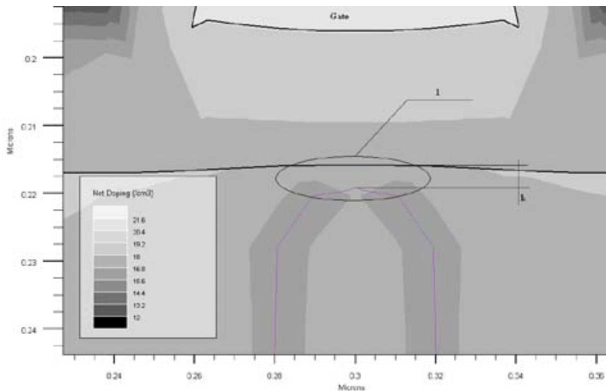

Fig. 4. Fragment of the section of the structure of the NMOS transistor with lateral implantation of impurities depends when the P implantation dose is 4x10^{13} cm^{-2}, and energy 35 keV.

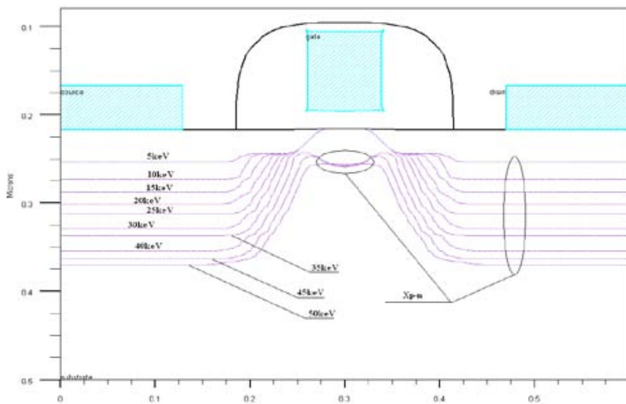

Fig. 5. Dependency of the *pn* depth of the simulated structure of the NMOS transistor with lateral implantation of impurities on the energy for the implantation of As ions when the ion dose is 1x10^{16} cm^{-2}

In the second case (with local side "pocket" formation) the II simulation results of the NMOS structure n^- area formation are presented in Fig. 6. and Fig. 7. In this case, during the implantation of P it is important not to exceed 30 keV in the entire dose range since the channel is not yet destroyed then. However, like in the first case, when the amount of energy is increasing in the NMOS structure, the overlapping with the gate areas is increasing and this increases the parasitic volumes of the structure. During the As II it is important not to exceed 35 keV in the entire dose range – then, the *L* is maintained. During the introduction of As impurities at a high dose of ions at maximum energy values the underrun of impurities under the gate reaches the depth of 30 nm, Fig. 7.

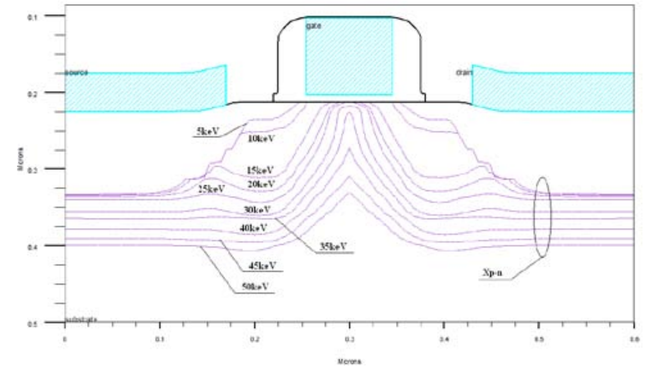

Fig. 6. Dependency of the *pn* depth of the structure of the NMOS transistor with local lateral "pocket" formation on the energy for the implantation of P ions when the ion dose is 1x10^{14} cm^{-2}

According to the variations of the simulated structures the transistor's output characteristics have the standard nature of change. However, in this case, it id more important to analyse the characteristics of gradient changes. In Fig. 9 we see the evolution of the saturation current in the simulation of the transistor II modes. We see that increasing the channel, the NMOS transistor saturation currents increase as well. In addition, it should be noted that with the NMOS channel less than 90 nm the saturation current ranges from 0.45 mA to 4.5 mA.

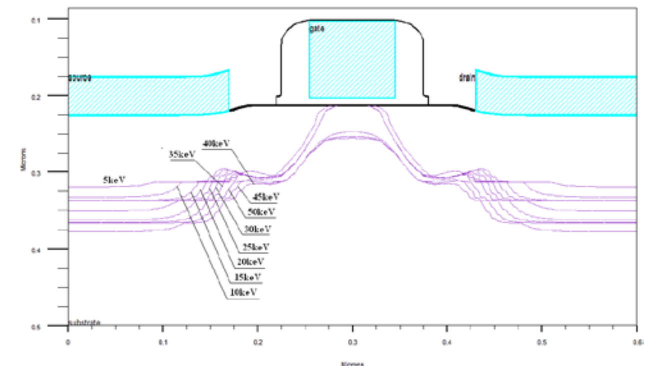

Fig. 7. Dependency of the *pn* depth of the structure of the NMOS transistor with local lateral "pocket" formation on the energy for the implantation of As ions when the ion dose is 1x10^{16} cm^{-2}

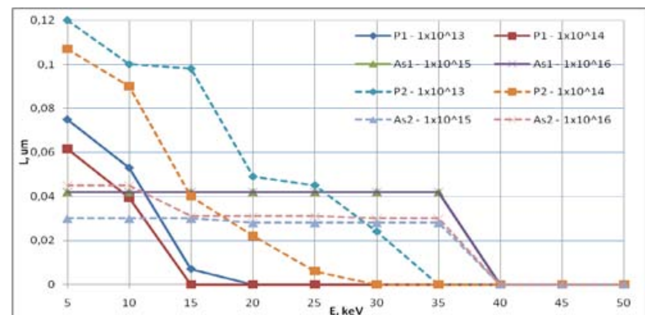

Fig. 8. *L* changes of the NMOS transistor with local "pocket" formation and NMOS transistor with lateral implantation of impurities depending on the II energy and dose. (Pi – the i-th type NMOS P implantation, Asi – the i-th type NMOS As implantation)

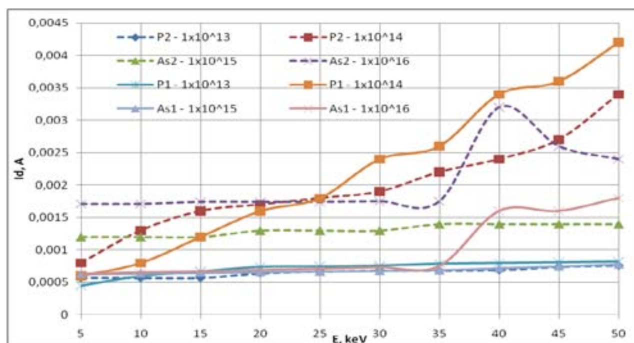

Fig. 9. Saturation current changes of the NMOS transistor with local "pocket" formation and NMOS transistor with lateral implantation of impurities. (Pi – the i-th type NMOS P implantation, Asi – the i-th type NMOS As implantation)

Conclusions

1. The structure with the lateral introduction of impurities is more sensitive to the n^- area formation II TO modes. At ion doses from $1x10^{13}$ cm^{-2} to $1x10^{14}$ cm^{-2}, the active induced *L* remains at only 5 keV and at 10 keV. Alternatively, the impurity underrunning under the thin gate oxide is observed.

2. For the NMOS transistor with local side "pocket" formation in the n^- area formation in the II method the TO energy in the entire range of implantation doses can not exceed 30 keV. Upon exceeding it, the induced channel *L* is destroyed.

3. In the formation of the main drain and source areas, n^+ we see that in the selected As II dose range *L* does not change as long as the energy does not exceed 40 keV. If exceeded, the impurities underrun under the thin gate. Then we can consider that the installed channel was formed with a depth of up to 30 nm for both NMOS simulated cases.

4. During the As implantation the active channel length *L* remains stable in a larger range of the II energy.

5. The simulations showed that when the ion implantation dose and energy are increased, the NMOS transistor's saturation current increases, which in the NMOS channel less than 90 nm varies from 0,45 mA up to 45 mA.

References

1. **William R.** Tonti, MOS technology drivers // IEEE Transactions on Device and Materials Realiability. 2008.
2. **Gary S. May., Costas J. Spanos.** Semiconductors manufacturing and process control. – A. John Wiley & Sons, INC., Publication, 2006. – 480 p.
3. Mathematical simulation programs ATHENA and ATLAS. Official Website of Silvaco International. Online: http://www.silvaco.com [10/01/2010].
4. **Keršys T., Anilionis R., Eidukas D.** Simulation of Doped Si Oxidation in nano–dimension Scale // Electronics and Electrical Engineering. – Kaunas: Technologija, 2008. – No. 4(84). – P. 43–46.
5. **Andriukaitis D., Anilionis R.** Thermal Oxidation Process Influence to the Three–Dimentional Integrated Structures // Electronics and Electrical Engineering. – Kaunas: Technologija, 2009. – No. 8(96). – P. 81–84.
6. **Puidokas V., Marcinkevičius A. J.** Analysis of Digital audio D-class Power Amplifiers Characteristics // Electronics and Electrical Engineering. – Kaunas: Technology, 2010. – No. 2(98). – P. 41–44.

Received 2010 02 15

V. Kašauskas, R. Anilionis, D. Eidukas. Simulation of the MOS Transistors Structures Channel Technological Problems // Electronics and Electrical Engineering. – Kaunas: Technologija, 2010. – No. 10(106). – P. 139–142.

The MOS transistor channel structure depends on a number of technological processes. The main problem includes the channel shortening by applying additional impurity distributions in the source and drain areas, using the ion implantation technological operations (TO). In the process it is important to know and accurately determine the right ion implantation TO technological modes. During the simulation we identified the TO critical modes, distorting or breaking down the channel, of the drain and source area formation. Effects of ion implantation TO modes to the transistor output characteristics was identified. Ill. 9, bibl. 6 (in English; abstracts in English and Lithuanian).

V. Kašauskas, R. Anilionis, D. Eidukas. MOS tranzistorinių struktūrų kanalo technologinių problemų modeliavimas // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2010. – Nr. 10(106). – P. 139–142.

MOP tranzistorių kanalo struktūra priklauso nuo keleto technologinių procesų. Pagrindinės problemos yra kanalo trumpinimas taikant papildomą priemaišų paskirstymą ištakos ir santakos srityse, atliekant jonų implantacijos technologines operacijas (TO). Gamybos metu svarbu žinoti bei tiksliai nustatyti reikiamus jonų implantacijos TO technologinius režimus. Modeliavimo metu nustatyti dviejų skirtingų technologinių maršrutų NMOS tranzistorių santakos ir ištakos sričių formavimo jonų implantacijos TO kritiniai kanalą iškraipantys ar suardantys režimai. Nustatyta jonų implantacijos TO režimų įtaka tranzistorių išėjimo charakteristikoms. Il. 9, bibl. 6 (anglų kalba; santraukos anglų ir lietuvių k.).