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Research paper

Tunable pseudocapacitance fractional-order capacitor integrated in a 65 nm CMOS process

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ABSTRACT

This work presents a novel integrated design of a fractional-order capacitor of order 0.5 with an adjustable pseudocapacitance controlled by a DC bias voltage. The device was fabricated using the 65 nm TSMC CMOS process. The pseudocapacitance can be adjusted in the range from 39 to 87 nF/*sec*^0.5 by applying a serial DC bias voltage at the input terminal (from 0 up to 0.7 V), and from 39 to 57 nF/*sec*^0.5 by adjusting the bulk-source voltage (from 0 up to 0.9 V) available at an independent terminal. The maximum error of adjustment between the simulated and measured responses is 12%. The first tuning approach is advantageous for remote adjustment of specific applications from a preceding stage within the signal-processing chain, where the signal source itself provides the required DC control component. The operational frequency range spans two decades. The operational frequency bandwidth ranges approximately from 2 kHz to >500 kHz, varying with DC driving. Signal amplitudes up to 100–200 mV can be processed linearly without introducing significant distortion. Process-corner and temperature variation (from −40 °C to +40 °C) analyses indicate maximum parameter deviations of up to 10%. The size of the chip is comparable to that of common SMT components, with a cell layout area of 0.911×0.162 mm (0.148 mm^2). The application example of the electronically fractional-order RLC low-pass filter is presented, demonstrating a slope of -30 dB/dec and pole frequency adjustability between 22 kHz and 13 kHz through electronic tunability of the designed CPE.

1. Introduction

Fractional order (FO) circuits [1] have been beneficially used in many electronic and sensing applications, including biology and biomedicine [2–4], food quality assessment [5,6], food safety [7,8], and many other areas. Fractional-order elements (FOEs) [1], considered both as physical circuit components and as mathematically defined impedances [9], have a significant impact on circuit theory. Their non-integer order enables a balance between purely resistive or capacitive (or eventually, inductive) behavior, giving rise to a variety of interesting phenomena. These properties enable novel approaches to control [10–12], compensation [13], and electronic adjustment [14] in practical applications. Moreover, the fractional nature of the elements can also facilitate an extension of the achievable tuning range [14].

The impedance of a FOE with capacitive behavior is defined as $Z_{C\alpha}(s) = 1/(s^{\alpha}C_{\alpha})$. The parameter α denotes the FO of the impedance ($0 < \alpha < 1$), while C_{α} represents the pseudocapacitance, measured in units of F/sec$^{1-\alpha}$. A fractional-order two-terminal device is also known as a constant phase element (CPE), as defined by Morrison and Valsa [15–17]. The theoretical phase of such an element lies in the range $-90° < \varphi_{\alpha} < 0°$ and is directly related to the order according to $\varphi_{C\alpha} = -\alpha \cdot 90°$ The ideal FO impedance has a frequency-independent phase. The magnitude of the impedance is defined as $|Z_{Ca}(f)|$ [dBΩ] $= -\alpha \cdot 20 \cdot \log(f) + 20 \cdot \log(1/(2\pi C_a))$.

In many recent studies [18–27], the tunability of circuit applications has not been provided by the FOE itself, but rather by other circuit features. This approach is frequently based on the parameters of active elements [20–27]. Although several works enabling intentional

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variation of FOE features, such as pseudocapacitance, order or both, have been published [18–30], most of them employ active implementations with multiple active devices [20,22–24,27]. Such solutions inherently suffer from additional power consumption and various limitations related to operating frequency, dynamic range, accuracy, and linearity [18–27].

Adjustable passive solutions [18,28–30] represent a quite new idea in this field. Early non-adjustable realizations were based on material-layer or liquid-based technologies, in which distributed RC networks are formed using layered structures [18,31], liquids [32], nanocomposites [33], or carbon nanotubes [34]. However, many of these approaches do not support dynamic and continuous adjustability. More recent pioneering works [28,29] have presented the possibility of electronically adjusting pseudocapacitance values. However, all of these solutions using discrete elements, which significantly limits their compactness and practical integration as a single solid-state device or a small chip. Therefore, this work has the following objectives:

a) a fully integrated fractional-order capacitor with tunable pseudocapacitance, enabling a compact package comparable to a surface mounted technology (SMT) device or smaller than solid-state passive FOEs [31–34] and standard discrete RC solutions [16,17,19,28,29],
b) pseudocapacitance adjustability at a fixed fractional order via a serial DC bias voltage,
c) pseudocapacitance adjustability at a fixed fractional order via an independent control terminal,
d) no or very low power consumption,
e) an operational frequency range spanning at least two decades, from units of kHz up to hundreds of kHz,
f) a pseudocapacitance range that yields impedance magnitudes lower than those typically available at active device terminals when used in circuit synthesis and design, thereby ensuring minimal loading and impact on active device terminals.

Based on an analysis of recent solutions available in the literature, no existing solution allows all of the abovementioned objectives simultaneously. However, these features are highly desirable in a wide range of many applications, including adjustable fractional-order circuits and systems [14,35,36], as well as modeling and characterization tasks [37,38].

Adjustable CPEs are primarily intended for the design of adjustable applications in analog and mixed-mode electronics. The order of an ideal CPE determines the phase relationship between voltage and current at the two-terminal interface, and consequently also defines the slope of the impedance magnitude characteristic. In contrast, the pseudocapacitance determines the vertical position of the impedance magnitude response and can therefore be regarded as an analogy to the capacitance value of a conventional integer-order capacitor. Although both parameters are important, practical tuning of parameters in applications, such as adjustment of time constant, pole frequency or oscillation frequency, primarily requires variation of the pseudocapacitance. This is because the fractional order changes the phase as well as the pseudocapacitance simultaneously. The electronic adjustability of passive CPEs through pseudocapacitance control enables simple tuning of both passive and active circuits, including filter cutoff frequencies, time constants of integrators, differentiators, controller parameters [10–13,21–27], and oscillation frequencies of oscillators and signal generators [14,37,38]. In general, pseudocapacitance tuning directly modifies the effective time constants of the system, thereby providing the desired application-level tunability. In particular, combining passive CPEs with active circuitry based on operational amplifiers enables efficient electronic control of circuit parameters. Even a relatively narrow pseudocapacitance tuning range may be highly beneficial, since fractional-order elements often introduce nonlinear and highly sensitive dependences between the application parameters and the fractional-order element characteristics. As a result, substantial tuning effects can be achieved even with relatively small control-voltage variations.

Table 1 summarizes the most important parameters of selected designs from the literature. A detailed analysis of the results summarized in Table 1 indicates that existing solutions do not provide the possibility of adjusting pseudocapacitance either by means of an additional serial voltage applied directly to the impedance terminal (*i.e.*, through our signal source) or via an independent control terminal (in passive solution). The first approach enables device control directly from the signal source through its DC component. This feature can be advantageous, for example, when a preceding block in a signal chain controls the filter response by superimposing a DC component onto the produced signal. The second approach enables independent adjustment without affecting the signal path or impedance terminal in any way. The proposed solution uniquely combines both adjustment mechanisms. Furthermore, to the best of our knowledge, the presented design represents the first fabricated on-chip device based on R-MOS (MOS capacitor) sections with intentional adjustment for applications in fractional-order circuits and systems. Recent studies indicate that many passive fractional-order solutions do not provide systematic pseudocapacitance tuning at all. Existing adjustable approaches are typically based on active devices and therefore require additional power consumption, which is not necessary in the proposed design.

The impedance magnitude range was intentionally selected to remain below the typical terminal resistance of active devices. As a result, the proposed element can be readily integrated into active circuits and systems without significantly affecting the behavior of the CPE or the overall system performance. In addition, implementation as a compact chip cell substantially improves device miniaturization and practical applicability compared to conventional discrete-component solutions.

On the other hand, certain limitations must be considered. The achievable on-chip capacitance values are inherently restricted to the range of tens to hundreds of pF in order to be maintain a practically feasible chip area. Consequently, the lower operational frequency limit is constrained to range of hundreds of Hz. Other qualitative characteristics, such as the operational bandwidth and the achievable number of frequency decades, can still be influenced by the design methodology, including the selection of the number of sections and the corresponding component values.

2. Proposed CMOS CPE

Fig. 1 shows the RC-based prototype CPE used as the basis for the design of tunable solutions employing CMOS elements. The initial values of elements were obtained based on the Morrison-Valsa's approach [15–17]. The design specifications for the initial CPE topology were as follows. The nominal initial operational bandwidth of the original RC topology is targeted at three decades, ranging from units of kHz to hundreds of MHz, with a phase shift of $-45°$ (order $\alpha = 0.5$) and a pseudocapacitance $C_\alpha = 40$ nF/sec$^{0.5}$. The effective frequency range extends from 8 kHz to 4 MHz, with a phase ripple of approximately ± 2–$3°$. To meet these requirements, a four-section topology was selected, which is sufficient to achieve the intended performance. External parasitic capacitances are expected to influence the high-frequency operational limits due to their parallel contribution the C_p element. Given the very small values of C_p, the operational bandwidth of the fabricated device is therefore expected to be limited to two decades. In particular, external stray capacitances on the designed PCB are in the range of 2–5 pF. While the well-known topology shown in Fig. 1 provides the desired fractional-order behavior, it does not offer electronic adjustability of the key CPE parameters. To enable tunability, the capacitors were replaced with NMOS transistors, as shown in Fig. 2. The required capacitance values were used to determine the MOS transistor width-to-length (W/L) ratios according to [30,39–41]:

$$C_n \cong W_n \cdot L_n \cdot C_{gg}, \tag{1}$$

Table 1
The comparison of chosen electronically adjustable solutions of CPEs.

Solution	Numberofactive/passiveelements	Adjustablepseudovalue	Adjustableorder	Double – parameteradjustment	Independentterminalforpseudovalueadjustment	Independenceofpseudovalueontheorderverified	Typeofdrivingparameter	Approximateoperationalfrequencyrange(decades)	Testedpseudovaluerange/(drivingforcerangeforasingleparametercontrol)	MinimalsizecomparabletoSMTelement	Pseudovalueadjustabilityratio	Testedorderoffractional – orderelementorrange	Reducedornopowerconsumption	Lowimportanceofsignallevels	Typeofcomponentsinanexperiment	Verification	Figure ofmerit(FOM)
[18]	***	Yes	Yes	No	N/A	No	Voltages	4	N/A	Yes	-	0.82	Yes	N/A	IP	S	N/A
[20]	16/5	Yes	Yes	No	No	No	Voltages	2	N/A*	No	-	0.25, 0.5, 0.75	No	No	DA	M	N/A
[21]	3/2	Yes	Yes	No	No	No	Currents	2	N/A*	No	-	0.3, 0.5, 0.7	No	No	IA	S	N/A
[22]	8/2	Yes	Yes	No	Yes	Yes	Current	2	31.2→18.9 kH/sec$^{0.5}$	Yes	1.7	0.5	No	No	IA	M	0.68
[23]	8/2	Yes	Yes	No	No	Yes	Currents	2	7.8→78.2 pF/sec$^{0.2}$	No	10	0.2	No	No	IA	S	2.00
									24.6→2.5 kH/sec$^{0.2}$		9.8						1.96
[24]	11/2	Yes	Yes	No	No	No	Current	2	N/A*	No	-	0.1→0.9^{+}	No	No	IA	S	N/A
[25]	3/2	Yes	No	N/A	N/A	Yes	Currents	2	949→94.9 pF/sec$^{0.5}$	No	10	0.5	No	No	IA	S, M	4.00
[26]	2/23	Yes	No	No	No	Yes	Voltage	2	9.2→85.1 µF/sec$^{0.75}$	No	9.3	0.25, 0.5, 0.75	No	No	IA	M	< 1.00
									2→19.6 µF/sec$^{0.5}$		9.8						
									0.34→3.1 µF/sec$^{0.25}$		9.1						
									1.79→0.19 kH/sec$^{0.75}$		9.4						
									408→41 H/sec$^{0.5}$		10						
									68→6.5 H/sec$^{0.25}$		10.5						
[27]	9/2	Yes	Yes	No	No	No	Current	2	N/A*	No	-	0.33, 0.5, 0.67	No	No	IA	S	N/A
[28]	-/15	Yes	No	No	No	Yes	Voltage	3	46→464 µF/sec$^{0.75}$	No	10	0.25	Yes	Yes	DP	M	6.00
[29]	-/8	Yes	No	No	No	Yes	Voltage	1	15→109 µF/sec$^{0.5}$	No	7.3	0.5	Yes	No	DP	M	1.83
[29]	-/13	Yes	No	No	No	Yes	Voltage	1	654→138 nF/sec$^{0.5}$	No	4.7	0.5	Yes	Yes	DP	M	1.08
[30]	-/10	Yes	No	No	No	Yes	Voltage	3	7→14 nF/sec$^{0.5}$	Yes	2.0	0.5	Yes	Yes	IP	S	1.80
Fig. 2	-/10	Yes	No	Yes	Yes	Yes	Voltage	2	39→87 nF/sec$^{0.5}$	Yes	2.3	0.5	Yes	Yes	IP	M	2.30
									39→57 nF/sec$^{0.5}$		1.5						1.50

* Solutions that show examples of various orders and pseudovalues without specifying the adjustment range for each order are marked as N/A, this indicates that adjustment is possible, but there is no available data for comparison; ** Theoretical discussions of scalability.

$^{+}$ Discrete step of 0.1 (discontinuous adjustment).

*** A different approach is used (a distributed RC network based on the conductive layers available in the CMOS process).

Abbreviations in Table I: DA – discrete active, DP – discrete passive, IA – integrated active (CMOS), IP – integrated passive (CMOS); M – measurement, S – simulation

Figure of merit = (Approximate operational frequency range in number of decades × Pseudovalue adjustability ratio) × (A + B + C + D + E) / Number of active and passive elements; A-E are binary "1″ (advantage) or "0″ based on the availability of the "feature": A – electronic tuning of C_α, B – reduced/no power consumption, C – double parameter adjustment (two independent parameters for C_α adjustment), D – integrated/compact (minimized size), E – low importance of signal levels (good linearity); the higher number = better FOM, note that this FOM is a more comparative scoring metric than a universal or general ranking of the solutions in this area.

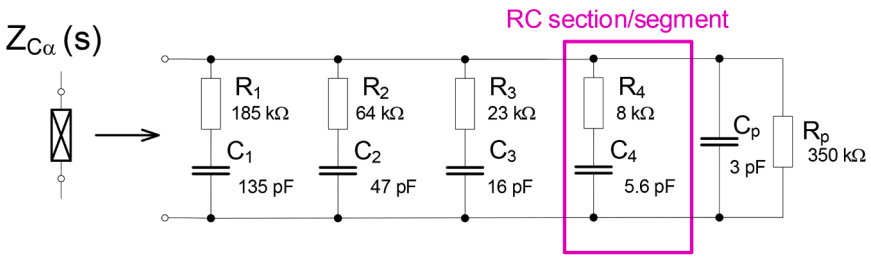

Fig. 1. Initial topology of the RC CPE solution used for further design of adjustable CPE.

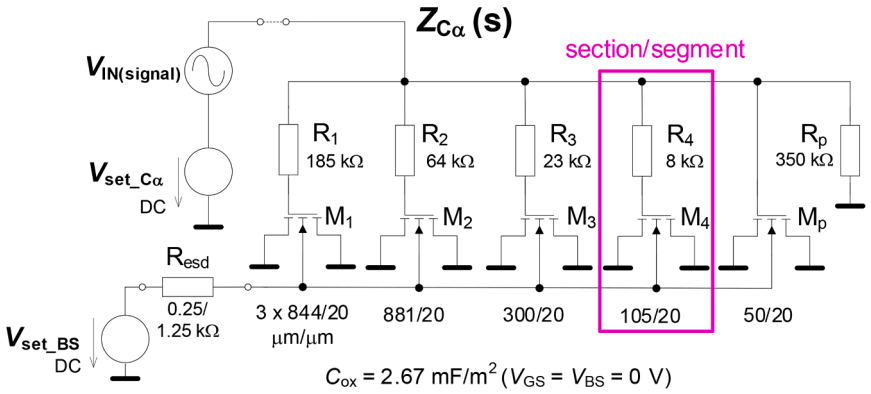

Fig. 2. The resulting topology of the CMOS adjustable CPE solution with both DC control voltages.

where n is the index of the corresponding transistor ($n = 1…k$), and C_{gg} is the gate capacitance (see Appendix), equal to 2.67 mF/m^2 ($V_{GS} = V_{BS} = 0$ V) for the employed CMOS process. This equation fits best the real verified capacity of MOS in our design.

The NMOS transistors used in the design operate as voltage-controlled capacitors (varactors) [29,39]. The applied DC voltage directly forms these capacitance values through resistors connected in series with the MOS gates; this the DC component of the applied control volage adjusts the pseudocapacitance value C_α of the CPE. In addition, the bulk-source voltage can also be used to tune C_α. However, the achievable tuning range is limited by the maximum allowable current through the bulk-source diode, since excessive current may lead to latch-up effects [39]. As a consequence, the bulk–source tuning method introduces power consumption associated with the driving voltage source (not from a supply voltage, since the circuit itself is passive and does not require a power supply). The resulting power consumption ranges from units of µW up to 500 µW within the specified V_{set_BS} tuning range. On the other hand, adjustment using the control voltage $V_{set\_C\alpha}$ does not introduce any additional power consumption. Therefore, the tuning effect of the voltage V_{set_BS}, on the C_α range is more limited than that of $V_{set\_C\alpha}$. Nevertheless, it provides a very simple control of C_α via a terminal that is independent of the impedance input terminal, which can be advantageous in certain applications [24–27]. It should be noted that the transistor bulks must be isolated from the basic substrate (a p-well in this case). Deep n-well isolation gap was therefore used in our design and particular CMOS process. Fig. 2 illustrates both possibilities of the pseudocapacitance C_α control based on two independent DC voltages.

In general, the proposed design can be provided for all values of fractional order between 0 and 1. However, changing the order requires a completely new set of RC values derived from the design algorithm presented in [15–17] for the initial RC prototype (see Fig. 1). Therefore, unlike pseudocapacitance, the fractional order cannot be adjusted systematically or continuously. Furthermore, there are practical physical limitations associated with the achievable element values [15–17,19]. Certain required component values may become either excessively small or excessively large, making them impractical for implementation using standard discrete components or even on-chip fabrication, where the available ranges of capacitance and resistivity are inherently limited.

The selected fractional order of 0.5, located at the midpoint of the achievable order range, represents a very good example and also favorable compromise that minimizes the influence of these implementation constraint [15–17,19], since it does not require inappropriate component values. In addition, the choice of order 0.5 corresponds to the square root operator in the time-domain, which is of considerable practical importance in applications involving integration and differentiation, such as controllers and filters. This feature is also demonstrated in the application example presented in Section 5, where a fractional order of 0.5 reduces the transition slope of a conventional first-order filter magnitude response from 20 dB/dec to 10 dB/dec. In the presented second-order filter, the corresponding slope is reduced from 40 dB/dec to 30 dB/dec.

3. Experimental results

The topology shown in Fig. 2 was implemented and fabricated using the TSMC 65 nm CMOS process (1.2 V voltage devices used). The following results compare traces obtained from Cadence Spectre simulations with experimental measurements of the fabricated prototype. The nominal AC sweep (compared to experimental results in this section) was set between 100 Hz and 10 MHz and parameters identical to experiments. The ESD protection resistor $R_{esd} = 200$ Ω and $C_{parasitic} = 1$ pF are connected in the input impedance terminal. Further simulation results, especially in Sections 4 and 5, have their specific simulation settings and variables discussed along with presented plots.

The example of impedance plots showing both magnitude and phase responses are presented in Fig. 3. These results demonstrate CPE behavior for the minimum and maximum values of the driving DC voltage $V_{set\_C\alpha}$ (0 and 0.7 V, respectively). The dependence of C_α on $V_{set\_C\alpha}$ closely follows the capacity dependence of the V_{GS} voltage of a single MOS transistor [30]. The adjustment of C_α is further captured in Fig. 4, which also shows the frequency ranges over which C_α remains flat (or minimally ripped) at both limits of the tested range. Fig. 4 shows the

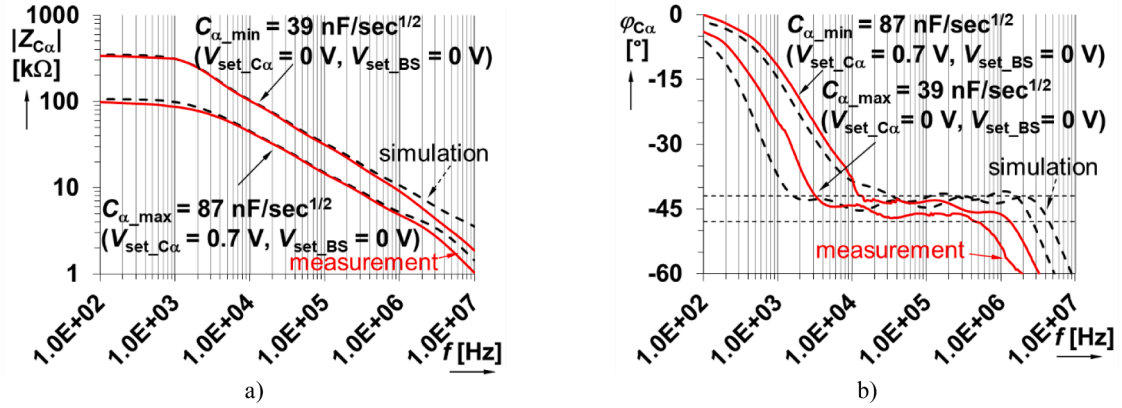

Fig. 3. The impedance plots of CPE impedance for typical $V_{set\_C\alpha}$ examples of an adjustment: a) Impedance magnitudes, b) Impedance phases.

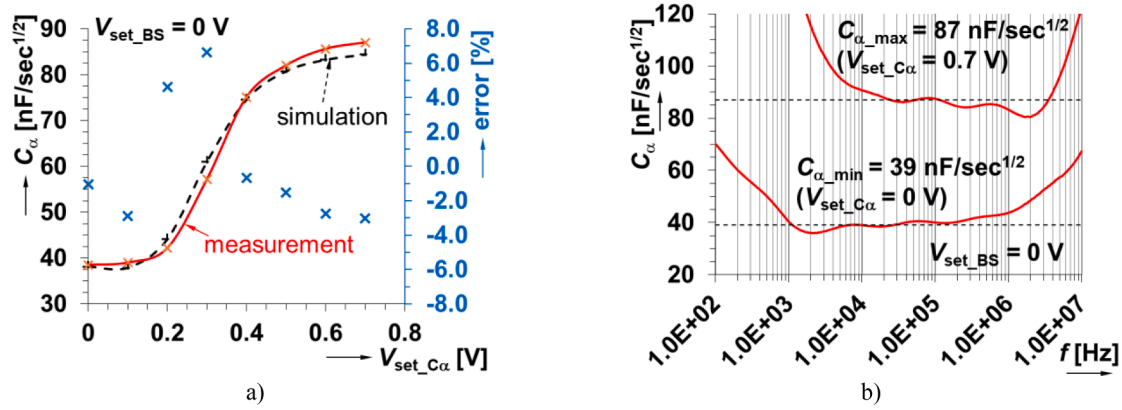

Fig. 4. The pseudocapacitance adjustability features: a) Dependence of C_α on the first driving voltage $V_{set\_C\alpha}$, b) The frequency range of stable C_α.

Table 2
The resulting parameters of the topology shown in Fig. 2.

n	R_n	M_n
1	185 kΩ → [W = 400 nm, L = 97.4 μm]	135 pF → 3 × [W = 844 μm, L = 20 μm]
2	64 kΩ → [W = 400 nm, L = 33.6 μm]	47 pF → [W = 881 μm, L = 20 μm]
3	23 kΩ → [W = 400 nm, L = 12.1 μm]	16 pF → [W = 300 μm, L = 20 μm]
4	8 kΩ → [W = 400 nm, L = 11.1 μm]	5.6 pF → [W = 105 μm, L = 20 μm]
p	350 kΩ → [W = 400 nm, L = 184 μm]	3 pF → [W = 50 μm, L = 20 μm]

error plot/points (with an error/deviation of up to 7%) between the simulated and measured $C_a = f(V_{set\_Ca})$ traces. Table 2 includes all technological parameters of fabricated CPE in detail. Table 3 compares the simulated and measured ranges of C_α values and the corresponding operational bandwidths. The phase ripple limits are ±3°. Differences observed in the bandwidth are primarily based on the initial underestimation of stray capacitances in parallel with M_p (*i.e.*, C_p). Nevertheless, the experimental results still satisfy the design requirement of a minimum operational bandwidth of two frequency decades in all cases. All experimental measurements were performed using a Keysight E4990A impedance analyzer with a source signal amplitude of 50 mV. The difference between simulated and measured C_α adjustment is <10%. The driving voltage is limited to 0.7 V because higher voltages do not result in further changes to C_α. This is consistent with the overall behavior of the C_{gg} capacitance as a function of V_{GS} voltage [30].

Bulk-source voltage control of C_α was tested as a complementary adjustment method. The corresponding results are shown in Fig. 5, with a numerical comparison provided in Table 4. Compared to $V_{set\_C\alpha}$, the achievable C_α tuning range is narrower in the case of V_{set_BS} (see Fig. 6). The difference between simulation and experiment in the impedance and phase plots is approximately 10–15%. After adjustment C_α (see Fig. 6), an error plot shows a maximum deviation of 12% between the simulation and the experiment. The maximum C_α value is reduced nearly by 30% relative to the $V_{set\_C\alpha}$. This reduction originates from the resistor R_{esd} (1.25 kΩ) required in the control terminal/node, as shown in Fig. 2. As R_{esd} approaches to 0 Ω, the tuning characteristic becomes exponential. However, such a configuration is not feasible, as the

Table 3
Comparison of the simulation (Expectation) and experimental results for C_a value adjustment by V_{set_Ca}.

Order (α)	0.5 (−45° ± 3°)	
Test	simulated	measured
$V_{set\_C\alpha}$ range [V]	0 → 0.7	
C_α range [nF/$sec^{0.5}$]	39.0 → 84.4	39.0 → 87.0
Ratio of C_α variation (max/min) [-]	2.2	2.3
Adjustability ratio (ratio of C_α / V_{bias} range)	3.1	3.3
Operational bandwidth range [Hz]	1.9 k → 3.31 M (0 V) 22.9 k → 4.37 M (0.7 V)	2.8 k → 0.57 M (0 V) 10.9 k → 1.51 M (0.7 V)
Ratio of operational bandwidth [-] (max/min)	1 743 / 190	204 / 139

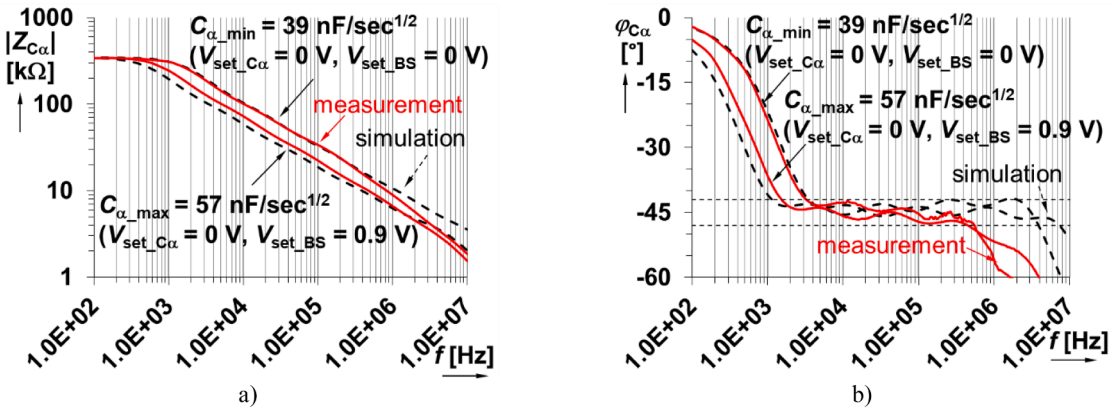

Fig. 5. The impedance plot of CPE impedance for the typical V_{set_BS} examples of adjustment: a) Impedance magnitudes, b) Impedance phases.

Table 4
Comparison of simulation (Expectation) and experimental result for C_a value adjustment by V_{set_BS}.

Order (α)	0.5 (−45° ± 3°)	
Test	simulated	measured
V_{set_BS} range [V]	0 → 0.9	
C_α range [nF/$sec^{0.5}$]	38.0 → 59.0	39.0 → 57.0
Ratio of C_α variation (max/min) [-]	1.6	1.5
Adjustability ratio (ratio of C_α / V_{bias} range)	1.8	1.7
Operational bandwidth range [Hz]	2.8 k → 7.58 M (0 V) 1.1 k → 4.30 M (0.9 V)	2.7 k → 0.53 M (0 V) 1.4 k → 0.60 M (0.9 V)
Ratio of operational bandwidth [-] (max/min)	2 707 / 3 910	196 / 429

resulting uncontrolled current could damage the BS diode and potentially trigger latch-up [39]. Although an additional series resistance is also present at the impedance input, its value is more than three orders of magnitude lower than the generated impedance magnitude, and its effect can therefore be neglected.

Fig. 7 presents a photograph of the device under test, including the designed PCB with auxiliary circuitry and measurement accessories, integrated within the package. Fig. 8 shows the layout of the proposed chip, which has dimensions of 0.911×0.162 mm (0.148 mm^2).

Due to the very limited number of chip samples, the repeated measurement uncertainty with various chip samples for statistical evaluation was not performed. However, the results of the process variations obtained in Cadence simulations (see Section 4) provide details about fabrication deviations and related uncertainties.

4. Characterization results of CPE under various conditions

The proposed CPE shown in Fig. 2 was analyzed via Cadence simulations to evaluate the influence of process variations and temperature changes. Since the proposed device is fully passive and does not require a power supply, no DC supply biasing is present. Consequently, the influence of supply-voltage variations does not need to be considered. The long-term stability of the proposed device was not analyzed. However, the maximum expected parameter deviations resulting from process variations are analyzed in the following subsections. Evaluation of long-term stability under continuous operation over periods of several weeks is planned as part of future work. Besides, the sensitivity of the device to variations in the tuning ("bias") voltages V_{set_Ca} and V_{set_BS} was tested. A ± 10% variation of both control voltages was applied at voltage corresponding to the highest tuning sensitivity of C_a, approximately 0.3 V for V_{set_Ca} and 0.5 V for V_{set_BS} (see Figs. 4 and 6). The resulting pseudocapacitance C_a variation was ±5 nF/$sec^{0.5}$ (±9% of the nominal value of C_a) for V_{set_Ca} and ±2 nF/$sec^{0.5}$ (±4% of the nominal value of C_a) for V_{set_BS}.

4.1. Process corners and temperature analysis of the designed CPE

Corner analysis was performed at room temperature (27 °C) using the standard worst-case process corners with the initial settings $V_{set\_Cα}$ = V_{set_BS} = 0 V. All process-corner simulations were performed using the standard typical–typical (tt), slow–slow (ss), fast–fast (ff), and skewed slow–fast (sf) and fast–slow (fs) process corners. Detailed descriptions of the corner models cannot be provided due to restrictions imposed by TSMC regarding the public disclosure of technology-specific parameters and process characteristics. The corresponding results are shown in

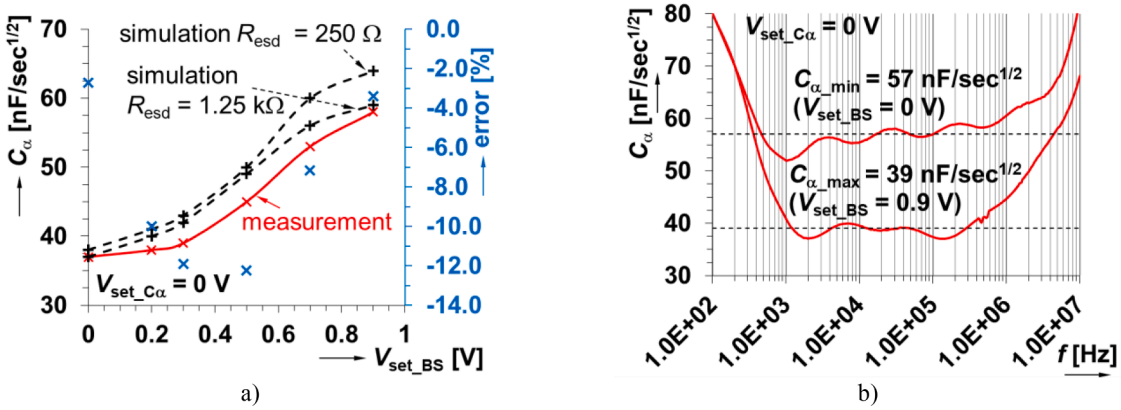

Fig. 6. The pseudocapacitance adjustability features: a) Dependence of C_α on the second driving voltage V_{set_BS}, b) The frequency range of stable C_α.

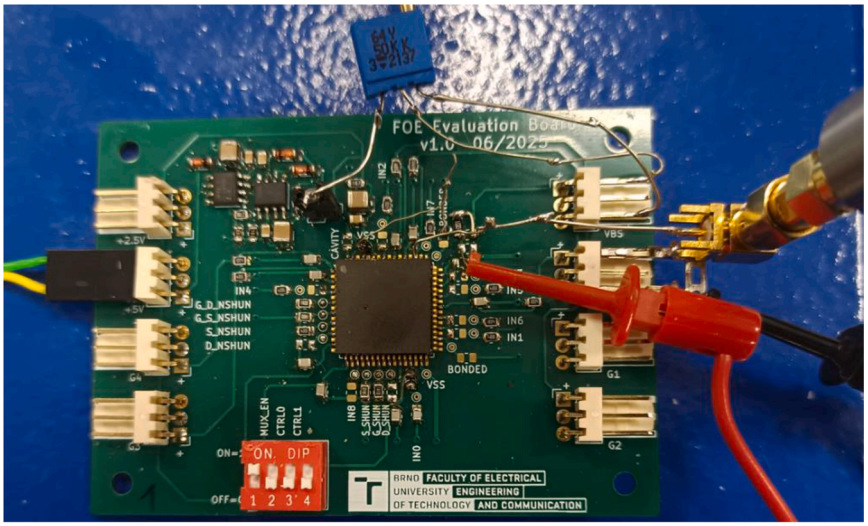

Fig. 7. The fabricated prototype and its measurement on a PCB.

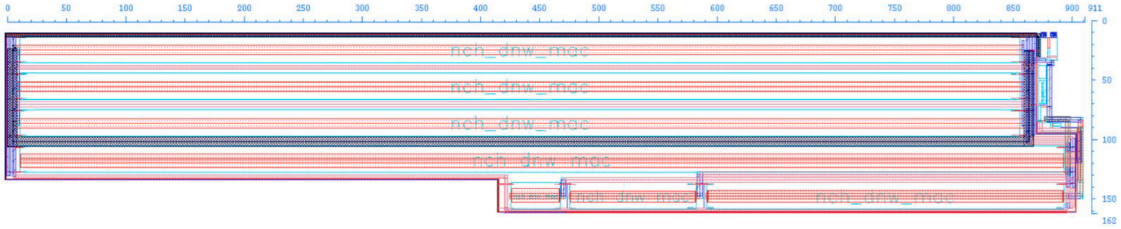

Fig. 8. The real layout of the CPE cell presented in Fig. 2 on the manufactured chip.

Fig. 9. These results indicate only a minor influence on the low-frequency impedance magnitude, with the impedance at 100 Hz varying between 295 kΩ and 350 kΩ, which results only in a slight shift of the operational band. Nevertheless, the phase response remains within the specified fluctuation limits of ±3°. At 100 kHz, the variation of the key parameters reaches approximately ±4 nF/sec$^{0.5}$ for the pseudocapacitance and ±0.2° for the phase response.

The results of the optimistic Monte Carlo process-variation analysis, consisting of 100 simulation runs assuming a normal distribution with 3σ spread, are shown in Fig. 10. In this case, the performance variation is significantly smaller than in the worst-case corner analysis, with the low-frequency impedance ranging from approximately 324 kΩ to 368 kΩ. Histograms plotted in Fig. 11 summarize the distributions of the key parameters, the pseudocapacitance and phase angle evaluated at the center of the operational bandwidth. The maximum pseudocapacitance deviation remains within ±4 nF/sec$^{0.5}$ from the nominal (mean) value, while the phase variation is limited to ±0.2° at 100 kHz.

Temperature sensitivity was evaluated over the range from −40 °C to +40 °C, and the corresponding results are shown in Fig. 12. This temperature range was selected to present the most common operating conditions expected for the proposed device in analog signal processing and communication systems. It covers temperatures above standard room temperature as well as sub-zero outdoor temperatures. The influence of the temperature appears to be even less significant than the previously discussed process variations. In fact, the resulting traces are so similar that Fig. 12 shows only detailed view of the responses to

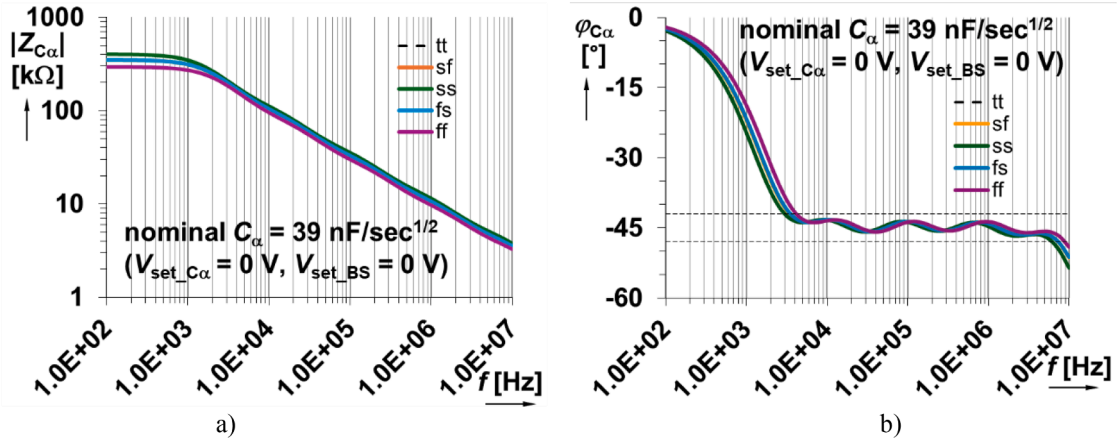

Fig. 9. Effect of hard corners on CPE performance: a) Impedance magnitude responses, b) Impedance phase responses.

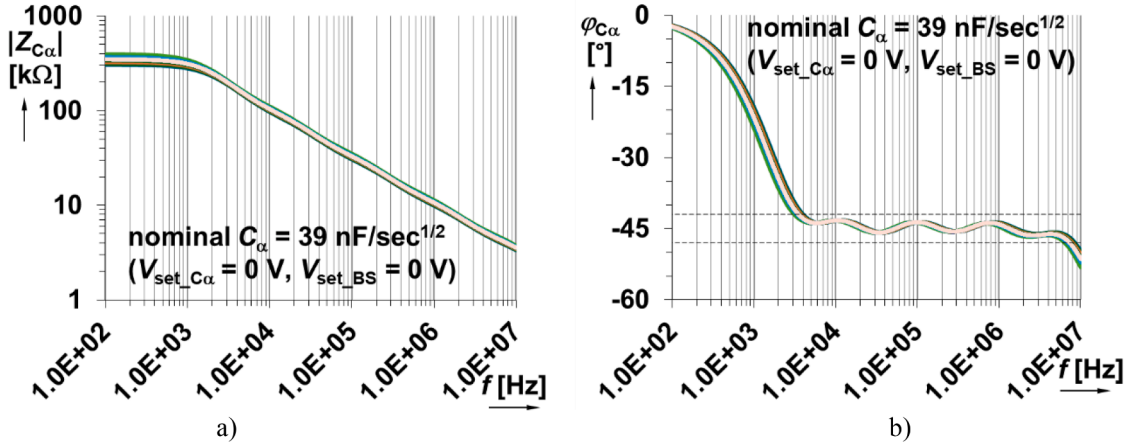

Fig. 10. Process variation effects on CPE performance (100 runs): a) Impedance magnitude responses, b) Impedance phase responses.

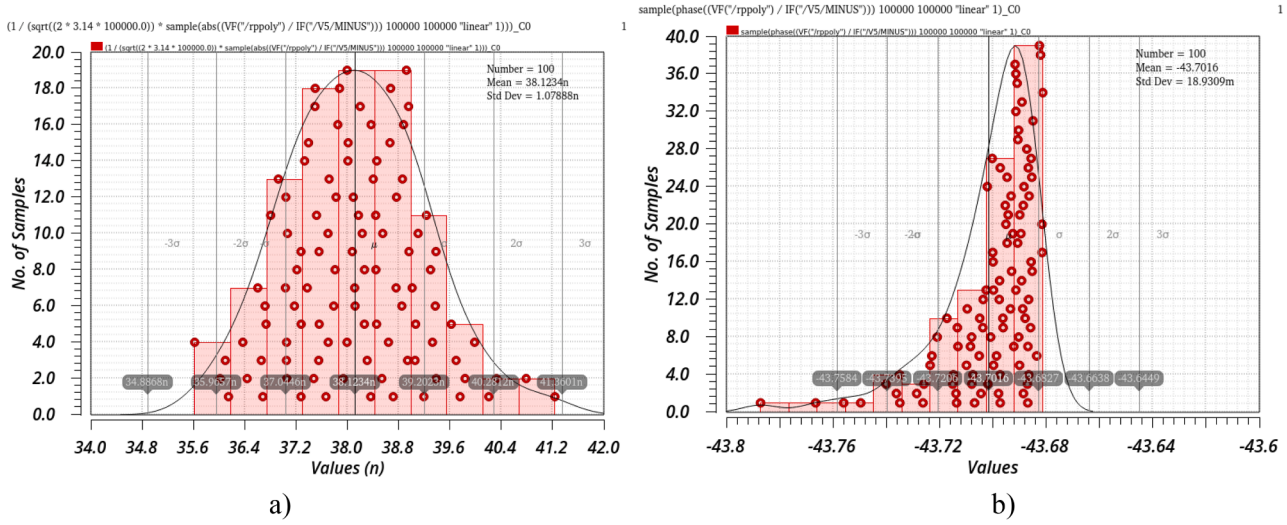

Fig. 11. Process variation effects on CPE performance: a) Histogram of pseudocapacitance, b) Histogram of phase.

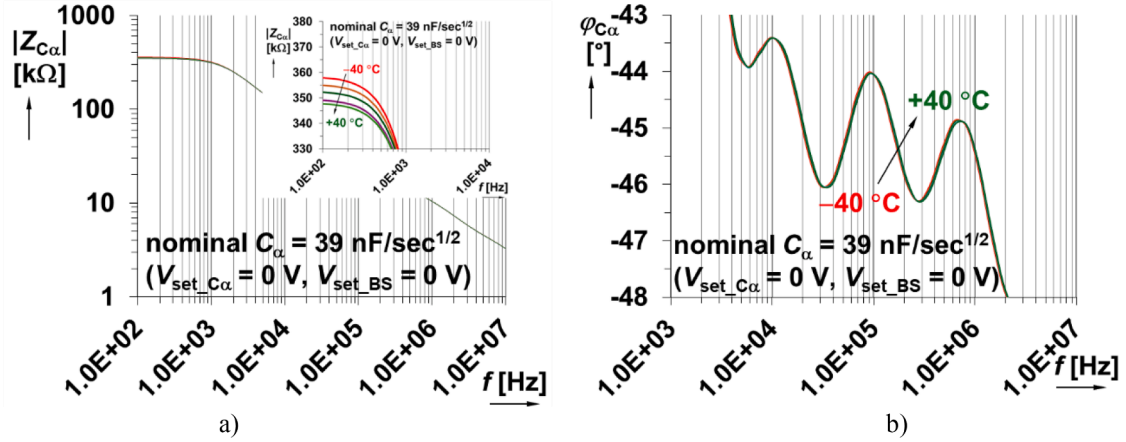

Fig. 12. Effects of temperature variation on CPE performance: a) Detail of impedance magnitude responses, b) Detail of phase responses.

highlight the differences. The variation of the low-frequency resistance is less than ±10 kΩ, specifically from approximately 348 kΩ to 358 kΩ). However, these deviations occur outside the intended operational frequency range of the CPE. Variations of the key parameters within the operational band are almost negligible: the pseudocapacitance changes by only about ±0.2 nF/sec$^{0.5}$, while the phase variation remains with approximately ±0.1°. This analysis shows significant robustness of the solution against temperature variation.

4.2. Nonlinearity of generated impedance

MOS devices are inherently nonlinear elements. Therefore, the signal amplitude plays a crucial role in their operation. This section explores the influence of the harmonic (sinusoidal) excitation amplitude on the linearity of the proposed CPE, evaluated through the current response by voltage excitation across the device. Voltage amplitudes across the CPE ranging from 10 mV to 300 mV (600 mV_{P-P}) were tested for the default configuration $V_{set\_C\alpha} = V_{set\_BS} = 0$ V. The corresponding results are shown in Fig. 13. Simulation-based explorations were performed for three frequencies: 1 kHz (the starting frequency of the operational range), 10 kHz, and 100 kHz. The results shown in Fig. 13 indicate that the maximum excitation amplitude ensuring sufficiently linear operation without distortion is approximately 200 mV for all tested cases. Example current waveforms are shown in Fig. 13(b). Results for 100 kHz are not included, since the impedance magnitude at this frequency is sufficiently low to provide even better linearity than at 1 kHz, making their presentation unnecessary.

The influence of DC tuning voltages $V_{set\_C\alpha}$, and V_{set_BS} on linearity was also explored. Both control voltages were tested independently at values of 0 V, 0.4 V, and 0.8 V, corresponding to the feasible tuning range limits. The results shown in Fig. 14 indicate that the applied control voltages primarily introduce a DC shift in the observed current, while having only a minimal effect on current linearity, distortion, and overall device performance. In particular, the phase angle remains within the intended ripple limits, while pseudocapacitance C_α is intentionally modified by the applied control voltage. The test frequency was set to 10 kHz and the excitation amplitude was set at the maximum linear operating value of 200 mV. At frequencies close to the lower edge of the operational band, the impedance magnitude increases significantly, current distortion becomes more significant. Therefore, under such conditions, the excitation amplitude should preferably remain below 100 mV, as demonstrated in the case of results obtained for 1 kHz (see Fig. 15). It should also be noted that no DC shift in the current is observed when the pseudocapacitance is controlled via V_{set_BS}, as shown in Fig. 14(b). In the context of this work, the nonlinearity limit is defined as the operating condition under which the total harmonic distortion (THD) of the output signal remains below limit of 5%. Distortion levels exceeding approximately 5% are readily observable in the time-domain waveform as illustrated in Fig. 13. In addition to THD, deviation of the measured A-V characteristic from the ideal linear response (represented by the red and black dashed lines) serves as an important indicator (criterion) of the onset of nonlinear behavior within specific regions of the operational bandwidth. It should be noted that THD evaluation can be affected by the finite bandwidth of the device, particularly when the test frequency approaches the upper limit of the CPE operational range. Under such conditions, higher-order spectral components may be attenuated differently, influencing the measured THD value. Therefore, the primary nonlinearity criterion adopted in this work is the deviation from the ideal linear A-V characteristic, which provides a consistent measure across all tested frequencies (1 kHz, 10 kHz, and 100 kHz).

4.3. Noise performance estimation

A simplified noise analysis was also performed to obtain an approximate estimate of the noise performance. It should be noted that accurate noise characterization is difficult in practice, since many additional factors beyond the proposed circuit itself, such as the PCB, interconnections, cables, and measurement instruments, can significantly influence the observed noise behavior. Therefore, the presented analysis is regarded only as an estimation.

The estimation focuses primarily on thermal noise contributions generated by the resistive elements in the CPE topology shown in Fig. 1, while the MOS elements are considered as capacitors from the small-signal perspective. The simulation-based results, shown in Fig. 16, indicate a maximum noise contribution of approximately 76 $nV/\sqrt{Hz}$ at low frequencies. The average noise spectral density, estimated as an approximate mean value between the minimum and maximum levels in Fig. 16, is around 30 $nV/\sqrt{Hz}$. Assuming a bandwidth of 10 MHz, this corresponds to an estimated effective noise voltage of 95 μV, which represents a peak-to-peak noise voltage of about 0.6 mV. Such noise levels are comparable to the hundreds of μV range that commonly occur in standard low-frequency analog systems. Based on this estimation, the resulting signal-to-noise ratio (SNR) exceeds 50 dB for an input signal with a peak-to-peak level 200 mV (corresponding to 100 mV amplitude). In practice, the SNR may vary substantially due to numerous secondary effects and commonly fluctuates within approximately ±10–20 dB, based on practical measurement setup.

5. Application example – tunable fractional-order RLC low-pass filter

To demonstrate practical applicability of the proposed CPE, a simple passive RLC low-pass filter topology shown in Fig. 17 was selected. The design requirements were a magnitude-response slope of −30 dB/dec and a stop-band phase shift of −135°. Such characteristics may be desirable in specific controller structures and analog signal-processing applications [10,11], but they cannot be achieved using conventional integer-order passive circuits, where only slopes of 20 dB/dec or 40 dB/dec are available for 1st and 2nd order passive filters, respectively. Moreover, this type of response cannot be realized using standard integer-order elements with electronic tunability. Therefore, the

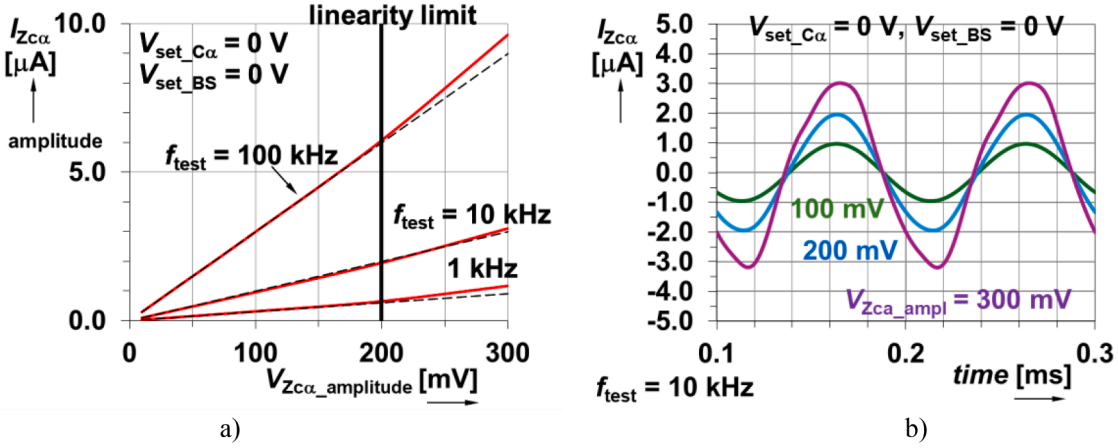

Fig. 13. Impact of applied signal voltage level on CPE linearity: a) Current through the CPE as a function of applied amplitude and frequency, b) Observed current waveforms at 10 kHz.

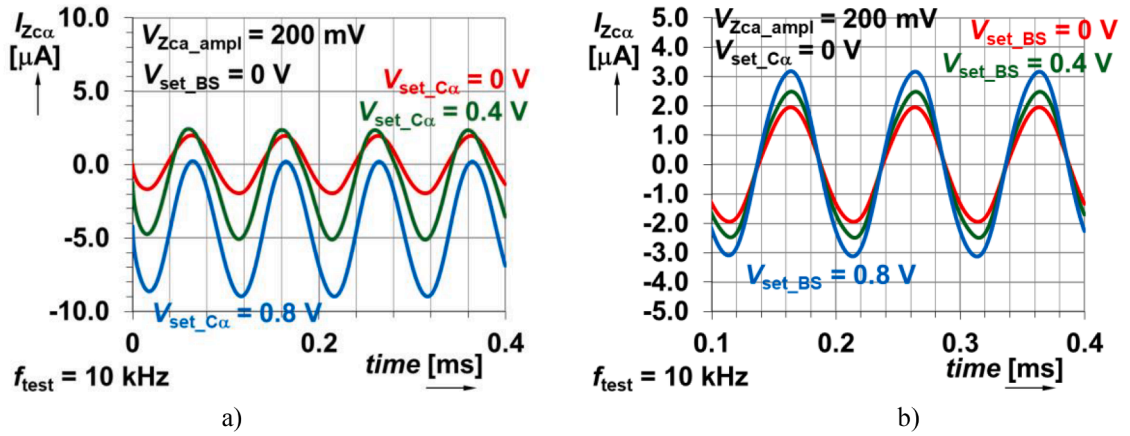

Fig. 14. Impact of applied DC driving voltages on CPE linearity (signal level 200 mV): Observed current waveforms at 10 kHz for: a) $V_{set\_C\alpha}$ and b) V_{set_BS}.

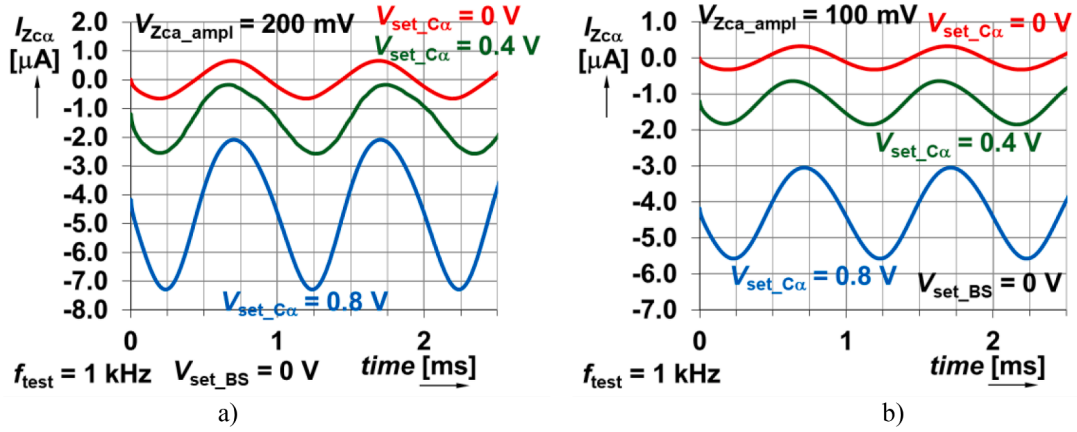

Fig. 15. Impact of applied DC driving voltages on CPE linearity for $V_{set\_C\alpha}$ adjustment observed for 1 kHz: a) Signal level 200 mV, b) Signal level 100 mV.

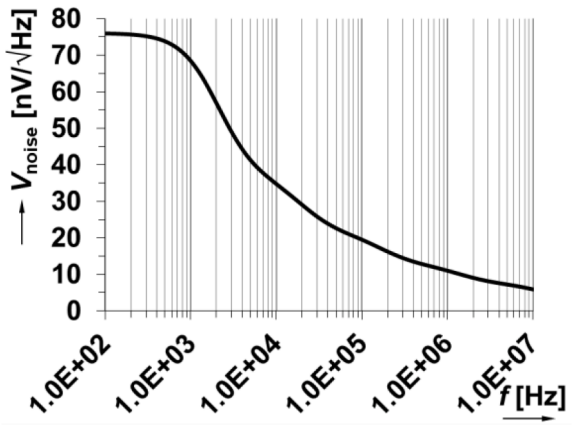

Fig. 16. The thermal noise density estimation from RC CPE in Fig. 1.

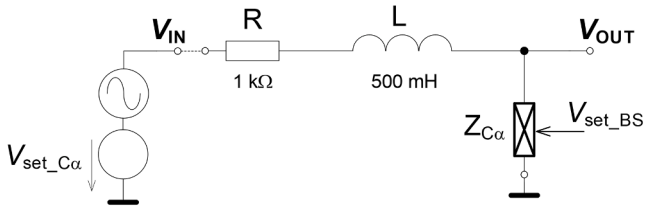

Fig. 17. Example of the proposed CPE application in a tunable RLC fractional-order filter.

proposed CPE provides an excellent illustrative example of a practical fractional-order application. The selected component values, $R = 1$ kΩ and $L = 500$ mH, were chosen to optimally match the operational frequency range of the proposed CPE, *i.e.* from units of kHz up to hundreds of kHz, while enabling pole frequency tuning within the range of tens of kHz. The selected inductance value is required to achieve the desired filter operating range in the kHz region. Such an inductor can be physically realized in two common forms. The first option is a conventional coil using a relatively thin wire on a ferromagnetic core. This solution is comparatively large, heavy, and bulky, and typically exhibits a series resistance of only a few tens of Ω. The second option is a compact molded or resistor-shaped inductor. This implementation occupies substantially less space and is comparable in size to standard through-hole technology (THT) resistor packages. However, its series resistance is typically higher, reaching a few hundred Ω. The parasitic series resistances of this order affect the quality factor of the filter by introducing additional losses. Nevertheless, in the proposed design, the influence of the series resistance of the inductor is partially masked by the dominant filter resistance (can be included to $R = 1$ kΩ) and has only a limited impact on the overall response. The voltage transfer function of the topology is:

$$K_V(s) = \frac{1}{s^{1+\alpha} C_\alpha L + s^\alpha C_\alpha R + 1}. \tag{2}$$

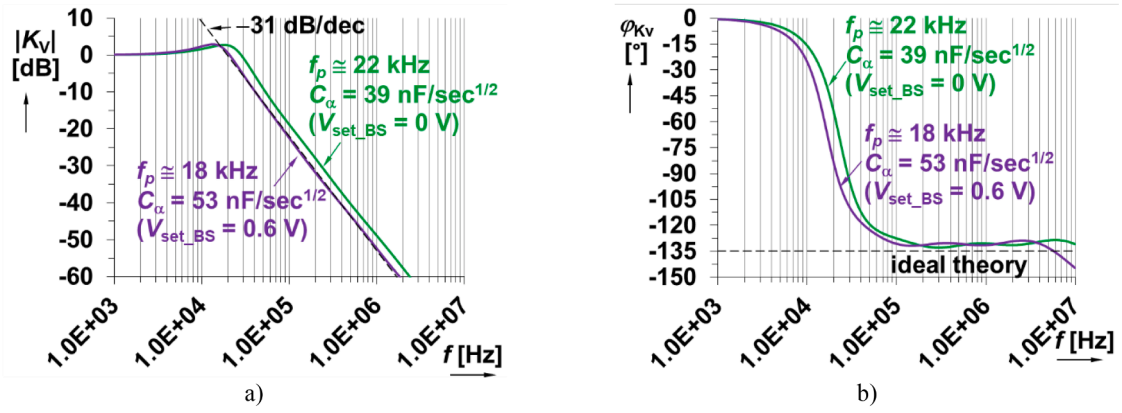

Fig. 18. Simulated fractional RLC filter voltage transfer responses when tuning is performed by V_{set_BS}: a) magnitude responses, b) phase responses.

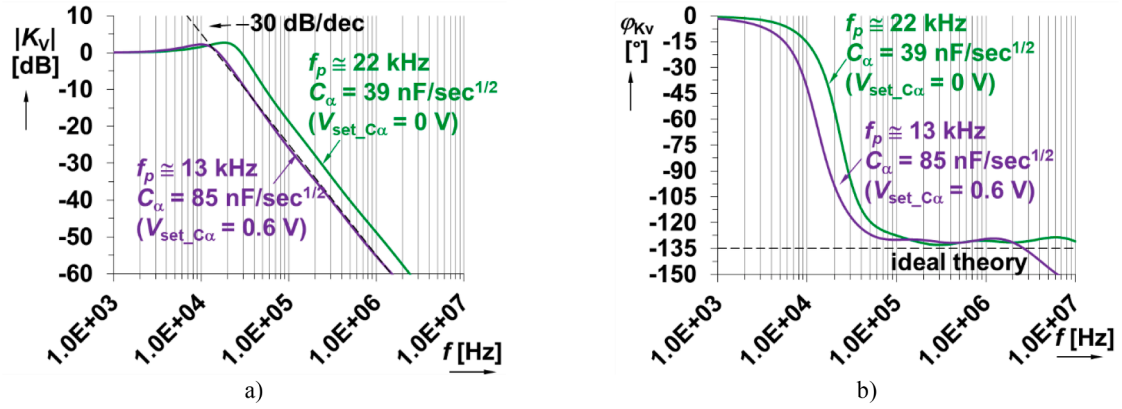

Fig. 19. Simulated fractional RLC filter voltage transfer responses when tuning is performed by $V_{set\_C\alpha}$: a) magnitude responses, b) phase responses.

From this expression, the pole frequency can be approximated as $\omega_p \cong (LC_\alpha)^{\frac{-1}{1+\alpha}}$. The selected CPE order $\alpha = 0.5$ fulfils the required magnitude slope and phase response, since a filter of order $1+\alpha$ exhibits a slope 1.5×20 dB/dec together with the desired high-frequency phase shift. Based on the previously discussed device characteristics, the pseudocapacitance C_α controlled by the voltage V_{set_BS} can be adjusted within the range of 39 and 59 nF/sec$^{0.5}$. For demonstration purposes, two control voltages $V_{set\_BS} = 0$ and 0.6 V, were selected, corresponding to $C_\alpha = 39$ and 53 nF/sec$^{0.5}$, respectively. This tuning range results in pole frequency adjustment from $f_p \cong$ 22 kHz down to 18 kHz. Cadence simulation results for the nominal process corner are shown in Fig. 18. The obtained magnitude slope reaches −31 dB/dec, while the stop-band phase shift is about −132°, both of which are in very good agreement with the intended specifications.

Furthermore, the existing DC-coupled signal path enables direct filter tuning through the signal source, or through the preceding section of the signal-processing chain. This feature represents a significant advantage, since the DC component of the processed signal can directly control the filter characteristics. In this operating mode, the achievable pole-frequency tuning range is wider because the pseudocapacitance adjustment using $V_{set\_C\alpha}$ provides a larger tuning range than bulk-source control. Specifically, the control voltages $V_{set\_C\alpha} = 0$ and 0.6 V correspond to $C_\alpha = 39$ and 85 nF/sec$^{0.5}$, respectively. Consequently, the pole frequency reaches from 22 kHz to 13 kHz, as shown in Fig. 19. The resulting magnitude slope remains close to −30 dB/dec, while the stop-band phase shift in is very similar to the previous case.

6. Conclusion

This work has introduced a novel CMOS-based implementation of an adjustable CPE device of order 0.5, operating over a bandwidth spanning from units of kHz up to hundreds of kHz. Although the practical experimental limits are influenced by the real parameters of the package and PCB, the realized device still achieves the targeted operational bandwidth of two frequency decades. Serial DC bias control provides a wider tuning range of and significantly higher adjustment accuracy with respect to theoretical predictions compared to bulk–source voltage control, whose precision is inherently limited by the behavior of the BS. Nevertheless, the availability of dual pseudocapacitance control offers important advantages for the application of FOEs in adjustable circuits, such as filters, oscillators, differentiators, and integrators used in control systems. In particular, bulk adjustment can be advantageous in scenarios where a DC component superimposed on the signal voltage at the impedance terminal is either not possible or not desirable. The presented application example based on a fractional-order passive RLC low-pass filter effectively demonstrates the intended functionality of the proposed CPE in analog implementations. Both tuning mechanisms were verified and compared. The filter pole frequency was electronically adjusted between 22 kHz and 13 kHz while maintaining the intended transition slope of −30 dB/dec between passband and stopband regions. The main results can be summarized as:

- Minimal compact size of the voltage adjustable fractional-order capacitor (0.148 mm^2),
- pseudocapacitance can be varied from 39 to 87 nF/sec$^{0.5}$ using a serial DC bias voltage adjustment (first control voltage) in the range of 0 to 0.7 V.
- pseudocapacitance range from 39 to 57 nF/sec$^{0.5}$ was achieved through bulk-source voltage adjustment (second control voltage) over the range of 0 to 0.9 V,

- resulting characteristics remain within the predefined acceptable limits up to a maximum deviation of 10% from nominal values,
- the maximum linear operating amplitude was found to be approximately 100 mV for tuning via $V_{set\_C\alpha}$ and about 200 mV for tuning via V_{set_BS},
- simulations predict noise levels in the range of several tens of nV/$\sqrt{}$Hz, which is typical for circuits of this type,
- the adjustable fractional-order filtering application example shows performance of presented solution.

Data availability

Key data of all results is provided within the manuscript. Supplementary data (datasets of computer-aided analysis of circuits and detailed measurement results) can be shared with readers based on their reasonable request (addressed to corresponding author).

Declaration of generative AI usage

During the preparation of this work, the author(s) used ChatGPT to help refine language and style. The author(s) reviewed and edited the content and take full responsibility for the publication.

CRediT authorship contribution statement

Roman Sotner: Writing – original draft, Visualization, Methodology, Investigation, Formal analysis, Conceptualization. **Jan Jerabek:** Writing – original draft, Supervision, Methodology. **Ladislav Polak:** Writing – review & editing, Writing – original draft, Visualization. **David Kubanek:** Writing – review & editing, Supervision, Methodology, Formal analysis. **Vilem Kledrowetz:** Writing – review & editing, Supervision. **Radek Theumer:** Writing – review & editing, Investigation, Conceptualization. **Darius Andriukatis:** Writing – review & editing, Supervision. **Alexandr Shadrin:** Writing – review & editing, Supervision, Methodology, Formal analysis. **Jan Dvorak:** Writing – review & editing, Supervision. **Dmitrii Semenov:** Writing – review & editing, Investigation, Conceptualization. **Pavel Horsky:** Writing – review & editing, Supervision, Methodology.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix

The proposed solution employs nonlinear MOS transistors as replacements for conventional capacitors [39–46]. Although such an implementation is feasible, it introduces several limitations that must be considered. The nonlinear behavior of MOS capacitances is well described in [39–44]. These nonlinear effects are typically significant under conditions involving large voltage and current variations, especially during switching operation, where the charge and voltage trajectories become strongly nonlinear. For example, [43] demonstrates highly nonlinear dependencies of C_{GS} and C_{GD} on V_{GS} for V_{DS} variations reaching tens or even hundreds of V. The operating conditions in the proposed design are substantially different. The device is intended for small-signal operation with voltage amplitudes in the range tens of mV, where these nonlinear effects are considerably less significant and can be omitted. The analysis presented in the paper confirms proper AC for signal amplitudes up to 100–200 mV.

In general, MOC capacitances can be modeled as the sum of an extrinsic parasitic component C_{ov} (overlap capacitance determined by geometry, permittivity, and technological constants) and an intrinsic voltage-dependent component C_{int}, associated with the MOS operating and regime and controlled by voltages such as V_{GS}, V_{BS}, and V_{DS} [39–42]. The total capacitance can therefore be expressed as $C_{gg} = C_{ov} + C_{int}$. Our case is specifically different from standard NMOS because drain, bulk and source electrodes are tied together. The overall gate capacity is defined as C_{gg} ($V_{GS} = V_{GD} = V_{GB}$) $= \frac{\partial Q_{Gtot}}{\partial V_{GS}}$, then $C_{gg} = C_{GS} + C_{GD} + C_{GB}$. For V_{GS} (V_G) < 0 V (accumulation region), the total capacitance approaches the oxide capacitance plus overlap component $C_{gg} = C_{ov} + W{\cdot}L{\cdot}C_{ox}$. In this region, the capacitance is essentially fixed and determined only by geometry and material parameters. For V_{GS} around 0 V and $0 < V_{GS} < V_{th}$ (below threshold), the channel is depleted and the oxide capacitance C_{ox} is now in series with depletion capacitance C_{dep}, i.e.: $C_{gg} = C_{ox}{\cdot}C_{dep}/(C_{ox} + C_{dep}) = C_{ox}/(1 + C_{ox}/C_{dep})$, where the depletion capacitance is given by $C_{dep} = \varepsilon_{Si}{\cdot}A/W_d$, with ε_{Si} denoting the permittivity of silicon, A the active area, and W_d the depletion layer width, which depends on V_{GS} [39–42]. For positive V_{GS} ($V_{GS} > V_{th}$, inversion) the transistor is in triode ($V_{DS} = 0$ V) region. Then C_{gg} is distributed between C_{GS} and C_{GD} ($C_{GB} = 0$) as: $C_{GS} = C_{GD} \approx 1/2{\cdot}W{\cdot}L{\cdot}C_{ox}$, then $C_{gg} = W{\cdot}L{\cdot}C_{ox}$. Note that literature (for example [39–42]) knows also formula for saturation ($V_{GS} > V_{th}$, $V_{DS} > V_{GS}$ - V_{th}) where C_{gg} dominant part is defined by $C_{GS} \approx 2/3{\cdot}W{\cdot}L{\cdot}C_{ox}$ but it is not accurate in our case (because $V_{DS} = 0$ V). Based on above discussions, our solution uses equation $C_{gg} \approx W{\cdot}L{\cdot}C_{ox}$ for calculation of initial values of CPE ladder capacitances (considering $V_{GS} = V_{GD} = V_{GB} = 0$ V). Note that in large processes or manual calculations, all of the capacities are considered constant, regardless of V_{GS}, V_{BS}, etc.

The influence of V_{GS} (where $V_{GS} = V_{GD} = V_{GB}$) on C_{gg} capacitance can be approximately expressed through the derivative of the total charge Q_{Gtot} with respect of V_{GD} (see Fig. 108 in [45]): $C_{gg} = \frac{\partial Q_{Gtot}}{\partial V_{GD}} \approx \frac{C_{ox}}{1+C_{ox}/C_s}$. The substrate capacitance C_S (or C_{dep}) itself depends on the substrate potential and therefore on V_{GD} [46]. However, the complete analytical expressions are highly complex and impractical for common engineering applications. Fig. A1 documents our discussion (W/L size 105 μm/20 μm, $C_{gg} \cong$ 5 pF for $V_{GS} = V_{GS} = 0$ V). The capacity changes between three modes of operation: accumulation (high value), depletion (low value) inversion (high value).

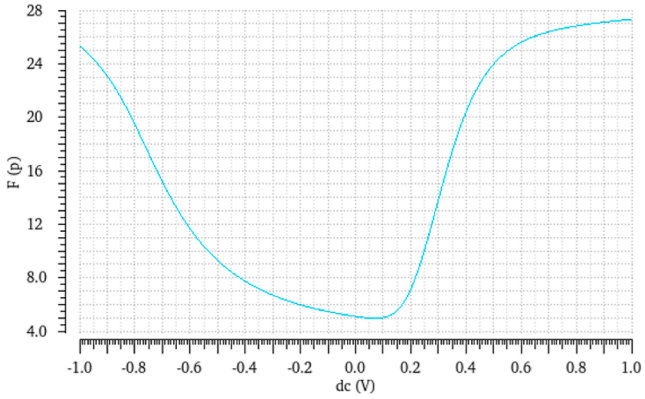

Fig. A1. Illustration of $C_{gg} = f(V_{GS})$ for 105 μm /20 μm NMOS.

The bulk voltage adjustment impacts the capacitance for weak and moderate forward bias of BS diode (where DC $V_{GS} = 0$ V and $V_{BS} > 0$ V). The bulk-source (body effect varying with threshold voltage) adjusts the capacity in weak bias conditions in accordance to $C_{gg} \approx C_{ox} \cdot C_{dep}/(C_{ox} + C_{dep})$ where $C_{dep} = \varepsilon_{Si} \cdot A/W_d$, with ε_{Si} denoting the permittivity of silicon, A the active area, and W_d the depletion layer width $W_d = \sqrt{\frac{2 \cdot \varepsilon_{Si}}{q \cdot N_A}(2 \cdot \phi_F - V_{BS})}$, where N_A is substrate doping, q is electron charge and ϕ_F is Fermi potential. The capacity rapidly increases when the BS diode becomes to strong forward bias (above 0.4 V in our case) and has exponential form defined by contribution of diffusion capacitance: $C_{gg}(V_{BS}) \approx \frac{\tau \cdot I_s}{V_T} e^{\frac{V_{BS}}{V_T}}$, where τ is carrier lifetime, V_T is thermal voltage and is junction saturation current [41,42]. The exponential increase is limited by maximal forward current (R_{esd} resistor in our case). As demonstrated in [30,39–46] the experimentally observed tuning characteristics obtained in this work are consistent with the theoretical behavior predicted by these models. Incorporating all the aforementioned mechanisms into the definition of pseudocapacitance C_α is not feasible and is not suitable for most engineers and designers. If necessary, we can only estimate some empirical constants, see for example [28].

References

[1] A.S. Elwakil, Fractional-order circuits and systems: an emerging interdisciplinary research area, IEEE Circuits Syst. Mag. 10 (4) (2010) 40–50, https://doi.org/10.1109/MCAS.2010.938637.

[2] T.J. Freeborn, A survey of fractional-order circuit models for biology and biomedicine, IEEE J. Emerg. Sel. Topics Circuits Syst. 3 (3) (2013) 416–424, https://doi.org/10.1109/JETCAS.2013.2265797.

[3] K.J. Wohlgemuth, T.J. Freeborn, K.E. Southall, M.M. Hare, J.A. Mota, Can segmental bioelectrical impedance be used as a measure of muscle quality? Med. Eng. Phys. 124 (2024) 104103 https://doi.org/10.1016/j.medengphy.2024.104103.

[4] C. Vastarouchas, C. Psychalinos, A.S. Elwakil, A.A. Al-Ali, Novel two-measurements-only Cole–Cole bio-impedance parameters extraction technique, Measurement 131 (1) (2019) 394–399, https://doi.org/10.1016/j.measurement.2018.09.008.

[5] A.M. Lopes, J.A.T. Machado, E. Ramalho, On the fractional-order modeling of wine, Eur. Food Res. Technol. 243 (2017) 921–929, https://doi.org/10.1007/s00217-016-2806-x.

[6] P. Ibba, et al., Bio-impedance and circuit parameters: an analysis for tracking fruit ripening, Postharvest Biol. Technol. 159 (2020) 110978, https://doi.org/10.1016/j.postharvbio.2019.110978.

[7] J. Slay, et al., Distinguishing liquid solutions with alcohol using electrical impedance measurements: preliminary study for food safety applications, IEEE Sens. J. 23 (22) (2023) 26997–27007, https://doi.org/10.1109/JSEN.2023.3315798.

[8] A.C. Patil, A. Fernandez la Villa, A.K. Mugilvannan, U. Elejalde, Electrochemical investigation of edible oils: experimentation, electrical signatures, and a supervised learning–case study of adulterated peanut oils, Food Chem. 402 (2023) 134143, https://doi.org/10.1016/j.foodchem.2022.134143.

[9] I. Podlubny, Fractional Differential Equations, Academic Press, San Diego, CA, USA, 1999.

[10] T.K. Bashishtha, V.P. Singh, U.K. Yadav, U.K. Sahu, Fractional-order PID controllers and applications: a comprehensive survey, Annu Rev. Control 60 (2025) 101013, https://doi.org/10.1016/j.arcontrol.2025.101013.

[11] I. Petráš, Fractional-order controllers: a practical approach, IEEE Trans. Syst. Man. Cybern.: Syst. 55 (12) (2025) 9570–9579, https://doi.org/10.1109/TSMC.2025.3614290.

[12] J. Nako, A.S. Elwakil, C. Psychalinos, Implementation and behavior of basic filters involving the delay element $\sqrt{(\tau s)}$, Circuits. Syst. Signal. Process. 44 (5) (2025) 3659–3671, https://doi.org/10.1007/s00034-024-02966-x.

[13] J. Nako, C. Psychalinos, F. Khateb, A.S. Elwakil, Bilinear double-order filter designs and application examples, IEEe Access. 12 (2024) 14040–14049, https://doi.org/10.1109/ACCESS.2024.3357092.

[14] R. Sotner, et al., On the performance of electronically tunable fractional-order oscillator using grounded resonator concept, AEU – Int. J. Electron. Commun. 129 (2021) 153540, https://doi.org/10.1016/j.aeue.2020.153540.

[15] R. Morrison, RC constant-argument driving-point admittances, IRE Trans. Circuit Theory 6 (3) (1959) 310–317, https://doi.org/10.1109/TCT.1959.1086554.

[16] J. Valsa, P. Dvořák, M. Friedl, Network model of the CPE, Radioengineering 20 (3) (2011) 619–626.

[17] J. Valsa, J. Vlach, RC models of a constant phase element, Int. J. Circuit Theory Appl. 41 (1) (2013) 59–67, https://doi.org/10.1002/cta.785.

[18] D. Kubanek, A. Shadrin, P. Seda, et al., Design, synthesis and simulation of fractional-order element using MOS transistors as distributed resistive capacitive devices, Sci. Rep. 15 (2025) 14717, https://doi.org/10.1038/s41598-025-96539-w.

[19] J. Petrzela, Accurate constant phase elements dedicated for audio signal processing, Appl. Sci. 9 (22) (2019) 4888, https://doi.org/10.3390/app9224888.

[20] R. Sotner, et al., Synthesis and design of constant phase elements based on the multiplication of electronically controllable bilinear immittances in practice, AEU – Int. J. Electron. Commun. 78 (2017) 98–113, https://doi.org/10.1016/j.aeue.2017.05.013.

[21] P. Bertsias, C. Psychalinos, A.G. Radwan, A.S. Elwakil, High-frequency capacitorless fractional-order CPE and FI emulator, Circuits. Syst. Signal. Process. 37 (7) (2018) 2694–2713, https://doi.org/10.1007/s00034-017-0697-0.

[22] G. Tsirimokou, et al., Electronically tunable fully integrated fractional-order resonator, IEEE Trans. Circuits Syst. II, Exp. Briefs 65 (2) (2018) 166–170, https://doi.org/10.1109/TCSII.2017.2684710.

[23] S. Kapoulea, et al., Generalized fully adjustable structure for emulating fractional-order capacitors and inductors of orders less than two, Circuits. Syst. Signal. Process. 39 (4) (2020) 1797–1814, https://doi.org/10.1007/s00034-019-01252-5.

[24] S. Kapoulea, C. Psychalinos, A.S. Elwakil, A.G. Radwan, One-terminal electronically controlled fractional-order capacitor and inductor emulator, AEU – Int. J. Electron. Commun. 103 (2019) 32–45, https://doi.org/10.1016/j.aeue.2019.03.002.

[25] S. Kapoulea, et al., Realizations of simple fractional-order capacitor emulators with electronically-tunable capacitance, Integration, VLSI J. 69 (2019) 225–233, https://doi.org/10.1016/j.vlsi.2019.04.004.

[26] R. Sotner, et al., A single-parameter voltage adjustable immittance topology for integer- and fractional-order design using modular active CMOS devices, IEEE Access. 9 (2021) 73713–73727, https://doi.org/10.1109/ACCESS.2021.3081140.

[27] E. Emanovic, M. Vonic, D. Jurisic, C. Psychalinos, Digitally controlled fractional-order elements using OTA-C structures, Electronics. (Basel) 13 (11) (2024) 2066, https://doi.org/10.3390/electronics13112066.

[28] R. Sotner, S. Colburn, J. Jerabek, L. Polak, T. Freeborn, Electronically tunable pseudocapacitance for fractional-order (α = 0.25) passive element, Measurement 253 (2025) 117681, https://doi.org/10.1016/j.measurement.2025.117681.

[29] R. Sotner, C. Black, J. Jerabek, et al., Practical design of variable fractional-order capacitors with a single tuning feature using field effect transistors and variable capacitance diodes, Sci. Rep. 15 (2025) 21892, https://doi.org/10.1038/s41598-025-07319-5.
[30] D. Semenov, R. Sotner, J. Jerabek, R. Theumer, Gate-controlled 3.3 V CMOS transistor-based constant phase element design, in: Proc. Int. Conf. Appl. Electron. (AE), Pilsen, Czech Republic, 2025, pp. 1–6, https://doi.org/10.1109/AE66163.2025.11197785.
[31] P. Ushakov, A. Shadrin, D. Kubanek, J. Koton, Passive fractional-order components based on resistive-capacitive circuits with distributed parameters, in: Proc. 39th Int. Conf. Telecommun. Signal Process. (TSP), Vienna, Austria, 2016, pp. 638–642, https://doi.org/10.1109/TSP.2016.7760960.
[32] A. Adhikary, M. Khanra, S. Sen, K. Biswas, Realization of a carbon nanotube based electrochemical fractor, in: Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), Lisbon, Portugal, 2015, pp. 2329–2332, https://doi.org/10.1109/ISCAS.2015.7169150.
[33] D.A. John, S. Banerjee, K. Biswas, Nanocomposite material characterization of a solid-state fractional capacitor, IEEe Trans. Electron. Devices 67 (3) (2020) 1136–1142, https://doi.org/10.1109/TED.2020.2965432.
[34] A.S. Mohapatra, S. Sarkar, K. Biswas, Fabricating solid state fractional capacitor in the frequency range of mHz to kHz, IEEE Trans. Compon., Packag., Manuf. Technol. 11 (11) (2021) 2035–2038, https://doi.org/10.1109/TCPMT.2021.3107916.
[35] A. Adhikary, S. Sen, K. Biswas, Practical realization of tunable fractional order parallel resonator and fractional order filters, IEEE Trans. Circuits Syst. I, Reg. Papers 63 (8) (2016) 1142–1151, https://doi.org/10.1109/TCSI.2016.2568262.
[36] A. Adhikary, S. Choudhary, S. Sen, Optimal design for realizing a grounded fractional order inductor using GIC, IEEE Trans. Circuits Syst. I, Reg. Papers 65 (8) (2018) 2411–2421, https://doi.org/10.1109/TCSI.2017.2787464.
[37] A.S. Mohapatra, S. Zimmermann, K. Biswas, Designing fractional oscillator for sensing different types of lossy capacitors, IEEE Trans. Instrum. Meas. 72 (2023) 2002809, https://doi.org/10.1109/TIM.2023.3264030.
[38] A. Tapadar, D. Roy, A. Adhikary, Ripe stage detection and optimal ripe hours prediction of a banana using modified fractional order Colpitts oscillator, IEEE Trans. Instrum. Meas. 74 (2025) 9518609, https://doi.org/10.1109/TIM.2025.3565248.
[39] R.J. Baker, CMOS Circuit Design, Layout, and Simulation, 3rd ed., Wiley–IEEE Press, Hoboken, NJ, USA, 2010.
[40] B. Razavi, Fundamentals of Microelectronics, 3rd ed., Wiley, Hoboken, NJ, USA, 2021.
[41] R.F. Pierret, Semiconductor Device Fundamentals. Original US Edition, Addison-Wesley, MA, USA, 1996. Reading.
[42] S.M. Sze, K.K. Ng, Physics of Semiconductor Devices, 3rd ed., Wiley-Interscience, Hoboken, NJ, USA, 2006.
[43] N. Wang, J. Zhang, Nonlinear capacitance model of SiC MOSFET considering envelope of switching trajectory, IEEe Trans. Power. Electron. 37 (7) (2022) 7977–7988, https://doi.org/10.1109/TPEL.2022.3151776.
[44] M. Shintani, K. Oishi, Y. Nishitani, H. Takayama, T. Sato, Comprehensive MOSFET capacitance characterization based on charge trajectories, IEEe Trans. Electron. Devices 72 (7) (2025) 3758–3766, https://doi.org/10.1109/TED.2025.3572874.
[45] Agilent Technologies, Nonlinear device models (Volume 1) [Online]. Available, https://people.ece.ubc.ca/robertor/Links_files/Files/ICCAP-2008-doc/pdf/icmdl.pdf, 2008 (accessed May 17, 2026).
[46] D. Vasileska, MOS capacitors: theory and modeling. [Online]. Available: https://nanohub.org/resources/1598/download/mos_capacitors_ppt.pdf (accessed May 17, 2026).