ELECTRONICS AND ELECTRICAL ENGINEERING

ISSN 1392 – 1215 *2010. Nr. 2(98)*

ELEKTRONIKA IR ELEKTROTECHNIKA

MICROELECTRONICS

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MIKROELEKTRONIKA

Thermal Oxidation Process Influence to the V-MOS Structure

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Introduction

The relentless scaling of silicon chips has become the most common theme of the body of semiconductor process research over the last 20 years. CMOS technology still dominates as the most prominent technology [1]

The pressure to scale comes from two sources: one economic and the other engineering. Economically, if the size of a single chip can be shrunk, then more chips can fit on a wafer, and the economics of semiconductor production will improve. From an engineering standpoint, semiconductor chips are becoming ever more complex and the number of transistors in the average chip is increasing as new functions are integrated and developed [2].

Three-dimensional integrated circuit design and production brings a number of technical and economic problems in a very high integration technology. The most important problem – the design and production complexity is considered. In this case computer programs allowing design and make three-dimensional integrated circuits simulation is used.

The main aim of this paper is to simulate three-dimensional mathematical structures with mathematical software package using thermal oxidation process and to examine the selection of the three-dimensional integrated element in the three-dimensional integrated circuits [2–4]

Kinetics model

Thermally grown silicon oxide separates semiconductor elements. The area of element formation must be the same during all technological processes. Separation of V-MOS elements can be produced using local oxidation [5–7].

There are several proposed thermal oxidation kinetics descriptive models: Deal–Grove, Reisman, Han and Helms and Massoud. The core of latter three models consists of Deal–Grove model. They accurately describe the thin silicon oxide growth kinetics than the Deal–Grove model, but the Deal–Grove model is often applied thermal oxidation of a broad assessment of adaptation options and its simplicity.

Silicon thermal oxidation process can be described as a system of oxidants (gas) – silicon oxide – silicon wafer (Fig. 1). During thermal oxidation the silicon wafer is coated with a thin silicon oxide layer and is exposed by oxidants. Process speed depends on the thermal oxidation process technological regime. Oxygen moves from the gaseous phase to the interface "gas – oxide". The flux F_1 of oxidants describes the following

$$F_1 = h_G (C_G - C_S), \quad (1)$$

here h_G – the gas–phase transport coefficient; C_G – concentration of oxidant molecules in the bulk gas; C_S – concentration of oxidant molecules immediately adjacent to the oxide surface [8–10].

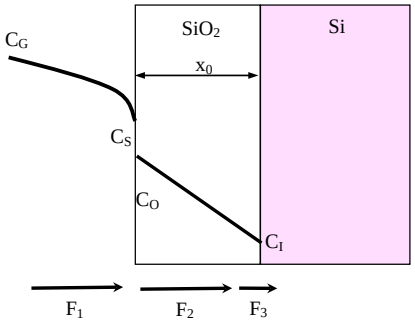


Fig. 1. SiO_2 growth kinetics model: C_G – concentration of oxidant molecules in the bulk gas; C_S – concentration of oxidant molecules immediately adjacent to the oxide surface; C_O – concentration of oxidant molecules at the oxide surface; C_I – concentration of oxidant molecules at the "SiO_2–Si" interface; x_0 – silicon oxide thickness; F_1 – flux of oxidant from gas to oxide; F_2 – flux through the oxide layer; F_3 – flux of oxidants consumed by the oxidation reaction at the oxide–silicon interface

Oxidant is absorbed and melts throughout the layer when the oxide surface is reached. In oxide oxidants solubility determines it's concentration gradient at interface "gas–oxide surfaces". Oxidants move from the interface "gas phase–SiO_2" to interface "SiO_2–Si". In this case, the flux of oxidants F_2 is proportional to the

difference of concentrations in oxide interfaces and inversely proportional to oxide thickness

$$F_2 = D\frac{dC}{dx} = D\frac{C_O - C_I}{x_0}, \quad (2)$$

here D – the oxidant diffusivity in the oxide; $\frac{dC}{dx}$ – a linear concentration gradient inside the oxide layer; C_O – concentration of oxidant molecules at the oxide surface C_I – concentration of oxidant molecules at the "SiO_2–Si" interface.

Reached the interface of "SiO_2–Si", oxidants begin to react with Si. As the result develops a new layer of SiO_2. Oxidation reaction rate describes the flux F_3 in the "SiO_2–Si" interface. Silicon oxidation is directly proportional to the flux of oxidants concentration

$$F_3 = K_S C_I, \quad (3)$$

here K_S – the surface rate constant.

These three fluxes (1–3) are equal in the steady state condition, which allows to express them as

$$F_1 = F_2 = F_3 = F = \frac{C^* K_S}{(1+\frac{K_S}{h}+\frac{K_S x_0}{D})} = \frac{HK_S P_G}{(1+\frac{K_S}{h}+\frac{K_S x_0}{D})}, \quad (4)$$

here P_G – the partial pressure of the oxidant molecules in the bulk gas.

The rate of oxide growth is proportional to the flux of oxidant molecules

$$R = \frac{F}{N_1} = \frac{dx_0}{dt} = \frac{HK_s P_G}{N_1(1+\frac{K_s}{h}+\frac{K_s x_0}{D})}, \quad (5)$$

here H – Henry's gas constant; N_1 – the number of oxidant molecules per cubic cm incorporated into the oxide layer; $h = h_G / HkT$; k – Boltzmann's constant; T – absolute temperature.

Assuming that at a time 0 the oxide thickness is x_0, the solution of this differential equation is of the form

$$\frac{dx_0}{dt} = \frac{B}{A+2x_0}, \quad (6)$$

$$(A+2x_0)dx_0 = Bdt, \quad (7)$$

$$x_0^2 + Ax_0 = B(t+\tau), \quad (8)$$

here $\tau = \frac{x_i^2 + Ax_i}{B}$; x_i – an initial oxide thickness $A = 2D\left(\frac{1}{K_S}+\frac{1}{h_G}\right)$; $B = \frac{2DHP_G}{N_1}$.

Solving the quadratic equation in regard of x_0 leads to the following expression for the oxide thickness in terms of oxidation time

$$x_0 = \frac{A}{2}\left(\sqrt{1+\frac{4B}{A^2}(t+\tau)} - 1\right). \quad (9)$$

In the long oxidation time ($t >> \tau$ and $t >> A^2/(4B)$), received

$$x_0^2 = Bt. \quad (10)$$

In the other limiting form oxidation time is short ($t << A^2/(4B)$), received

$$x_0 = \frac{B}{A}(t-\tau). \quad (11)$$

$\frac{B}{A}$ is called the linear rate coefficient and B is called the parabolic rate coefficient [5, 6, 10].

Thermal oxidation process can be described in a system of partial differential equations in the mathematical point of view.

Finite element method in the simulation of the process of local oxidation of silicon

Application of finite element method is conditioned by thermodynamic processes of oxidation, determined by molecules of Si, SiO_2 and oxidants. The method is widely applicable, because simulated structure can be presented both in two and three-dimensional space. It is seeked by this method to maintain the minimum transitional zone (usually the transition zone is limited by one element) [5, 11].

Calculation accuracy depends on the number of grid nodes in finite element method. Increasing the number of nodes, receiving larger data arrays demands more computing memory and increases the calculation duration. Main lack of the finite element method – there is a need to update finite element mesh after each time step, since a new layer of SiO_2 is formed. It is quite difficult to preserve the quality of the grid during the oxidation process simulation. To facilitate this task the SiO_2 domains are regrouped after each time step [5, 11, 12].

Simulation of mathematical structures

ATHENA program of mathematical simulation software package TCAD is used for mathematical structures simulation. It is adapted to the specific case of simulation using subprograms [13].

To ensure minimum impact on three-dimensional integrated element the local thermal oxidation must take place under conditions which allow the minimum deviation of characteristics of the integrated structures from the designed ones. Rational conditions of thermal oxidation process can be achieved with sustainable technological and structural parameters, such as oxidation time, temperature, thickness of silicon nitride mask and SiO_2 (P_{O2}=1 atm). Each of these parameters affects the type of LOCOS formation, stress distribution, lift-up nitride mask, lateral oxide under the silicon nitride mask, thin oxide form in the three-dimensional structures. Simulation was carried out in accordance with the model structure [5].

Mathematical models are created using the finite element method for local thermal oxidation process simulation [5].

It is important to avoid distortion of integrated elements in the three dimensional integrated circuits. In this case mathematical model is created (three-dimensional V–groove field effect transistor (V-MOS)) (Fig. 2).

The channel is formed in accordance with entire “V” perimeter in the V-MOSFET mathematical model. In the same area the three-dimensional structure of V-MOS mathematical model is formed, the channel length is up to 0,2 µm. The three-dimensional "V" groove depth is 0,739 µm and length – 0,521 µm.

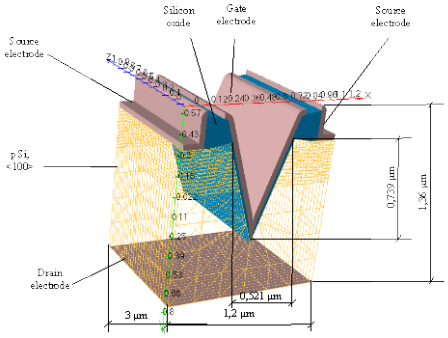


Fig. 2. V-MOS transistor mathematical model

The main problem in the thermal silicon oxidation process – diffusion impurities in the lower doped layers – leads to redistribution of diffuse areas and characteristics of the three-dimensional integrated structures.

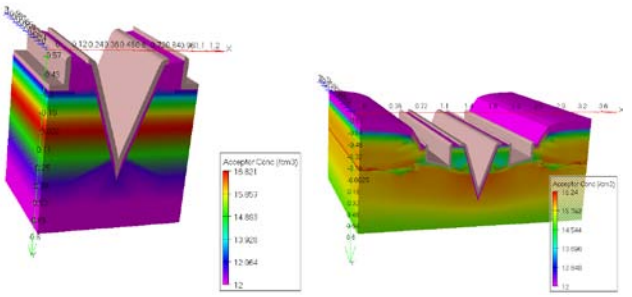
The parameters of three-dimensional integrated element and three-dimensional integrated structure change due to the thermal technology, which are difficult to identify and evaluate during the production. In this case the major human and material resources are required. That’s why a mathematical simulation of technological processes is used.

The simulation of three-dimensional structures conformation

The results of simulation have been carried out in the three-dimensional integrated structure simulation (Fig. 3, Fig. 4), when transistor (Fig. 2) is simulated between local oxides. However, for large number of technological operations it is impossible to form an ideal structure, what the result of mathematical simulation using the finite element method of three-dimensional structure of is substantially strained.

Three-dimensional V-MOS transistor is used in order to avoid regions redistribution and increase the escarpment of transistor characteristics. The drain current of the transistor determines the channel area, a three-dimensional V-MOS structures can be used to power integrated structures, light emitting busy diodes, indicators and even low-power engines. Another advantage of the three-dimensional V-MOS technology is the savings of about 40% of the area compare to three-dimensional NMOS technology [5].

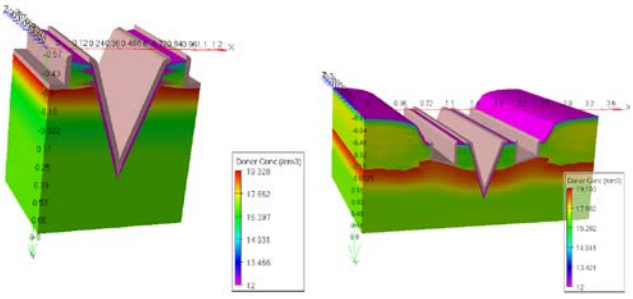
Using V-MOS less opportunities to redistribute impurities in source and drain regions appear during the thermal oxidation process, since the transistor drain current determine the length of the channel in the "V" shaped groove. According to the areas of redistribution in NMOS, the formation of a three-dimensional V-MOS in the three-dimensional structure is simulated (Fig. 3 and Fig. 4).



a) b)

Fig. 3. Acceptor concentration in three-dimensional structuress: a – in V-MOS transistor structure; b – in integrated with V-MOS transistor structure

In the case of impurity distribution and movement of pn areas it was received that the most impurities were redistributed after three-dimensional thermal oxide formation processes.



a) b)

Fig. 4. Donor concentration in three-dimensional structuress: a – in V-MOS transistor structure; b – in integrated with V-MOS transistor structure

It was found out that during the thermal oxidation process impurities move into the lower doped layers in the three-dimensional integrated structures.

The redistribution of acceptors and donors in much larger volume during the formation of three-dimensional integrated structure using the local oxidation process formation was received. This is the result of thermal oxidation. Here acceptors were redistributed below the "V" shaped groove. Possible solution – a deeper "V" groove, but in this way largest groove increases not only the depth, but also the width which reduce the degree of integration

Conclusion

1. The finite element method was used to create structures – the three-dimensional V–groove field effect transistor, which estimates redistribution of impurities

caused by thermal oxidation process in integrated three-dimensional structure.

2. Redistribution of impurities in the thermal process is very important for the production of three dimensional integrated structures of increasingly higher integration degree.

3. In the case of impurity distribution and movement of pn areas it was received that the most impurities were redistributed after three-dimensional thermal oxide formation processes.

4. It was found out that during the thermal oxidation process impurities move into the lower doped layers in the three-dimensional integrated structures.

5. It was obtained by simulation that the three-dimensional V-MOS technology saves about 40% of the area compare to three-dimensional NMOS technology.

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Received 2009 09 03

D. Andriukaitis. Thermal Oxidation Process Influence to the V-MOS Structure // Electronics and Electrical Engineering. – Kaunas: Technologija, 2010. – No. 2(98). – P. 45–48.

Problems of thermal oxidation process influence, related with V-MOS transistors separation was researched. Silicon thermal oxidation process described as a system using kinetics model. Three-dimensional integrated structures are formed using the finite element method for local thermal oxidation process simulation. Determinated, that parameters of "V" three-dimensional integrated element and three-dimensional integrated structure change due to the thermal technology, which are difficult to identify and evaluate during the production. Redistribution of impurities in the thermal process is very important for the production of three dimensional integrated structures of increasingly higher integration degree, impurities move to other areas or redistribute because of the thermal process, error occurs in the formed areas. It was obtained by simulation that the three-dimensional V-MOS technology saves about 40 % of the area compare to three-dimensional NMOS technology. Ill. 4, bibl. 13 (in English; summaries in English, Russian and Lithuanian).

Д. Андрюкайтис. Влияние процесса термического окисления на трехмерные интегральные структуры // Электроника и электротехника. – Каунас: Технология, 2010. – № 2(98). – С. 45–48.

Исследовано влияние процесса термического окисления на разделение транзисторных V-МОП структур. Проведено моделирование интегральных структур, применяя метод конечных элементов. Определено, что на параметры интегрального элемента и всей интегральной структуры влияют термические технологии, параметры которых довольно трудно определить при производстве. Перераспределения примесей после термических процессов наиболее важны при больших уровнях интеграции микросхем. Из-за этого возникают геометрические погрешности формируемых структур. При моделировании V-МОП технологий установлена возможность уменьшения площади на 40 % по сравнению с МОП. Ил. 4, библ. 13 (на английском языке; рефераты на английском, русском и литовском яз).

D. Andriukaitis. Terminės oksidacijos proceso įtaka V-MOP struktūroms // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2010. – Nr. 2(98). – P. 45–48.

Išnagrinėta terminės oksidacijos proceso įtaka V-MOP tranzistorių atskyrimui. Atliktas trimačių integrinių struktūrų modeliavimas baigtinių elementų metodu. Baigtinių elementų metodo taikymas sąlygojamas oksidacijos procese vykstančių termodinaminių procesų, kurie sieja *Si*, SiO_2 ir oksidanto molekules. Nustatyta, kad trimačio integrinio elemento su suformuotu vertikaliu „V" formos grioveliu ir trimatės integrinės struktūros parametrų kaitą lemia terminės technologijos, kurių poveikį sunku nustatyti ir įvertinti gamybos metu. Priemaišų persiskirstymas po terminio proceso turi labai didelę reikšmę gaminant vis didesnio integracijos laipsnio trimačius integrinius grandynus, nes dėl terminių procesų priemaišos difunduoja, persiskirsto, atsiranda formuojamų sričių paklaidų. Modeliuojant nustatyta, kad, taikant V-MOP technologiją, galima sumažinti integrinės struktūros plotą iki 40 %, palyginti su NMOP technologija. Il. 4, bibl. 13 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).