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Specific Features of Faults of Combinational CMOS Circuits

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Introduction

Additional problems arise because of increase of integration level and size of integral circuits during functionality modeling of such circuits and when performing fault analysis. A problem of adequacy of imitated higher-level faults to physical transistor faults emerges. This is particularly important in case of MOS and CMOS integral circuits, in which the number of transistors is close to the number of logical gates.

Transistor-based MOS and CMOS circuit is not always directly represented by logical model (only the function is reflected in most cases) or faults of logical model are not adequate to faults of transistor-based circuit. When equivalent logical scheme consists of many fictional elements or lines which are not present in transistor-based circuit, additional problems arise during processing of fault model.

Specific faults emerge because of discontinuities due to inner transistor capacitances in CMOS circuits. These faults are called parasitic. In this case additional logical elements are implemented in logical model subject to fault type.

Application possibilities of physical CMOS circuit transistor fault model and its adequacy to faults of logical scheme is analyzed in this paper. Comparative results are presented, which show how test sets by which function and logical scheme faults are detected can be applied to detect physical transistor faults.

Physical fault model of example combinational circuit

Functions, logical schemes and transistor physical faults of investigated examples are analyzed in this work. It is analyzed by which degree the tests, which are used to verify the function and logical scheme of selected example, are suitable for diagnostics of physical (transistor-level) faults of these schemes. Transistor-based circuit constant faults, short-circuiting, all faults input into the circuit and their detection level are distinguished. Conception of non-determined (X) faults characterizes the state when due to the fault intermediate signal (between logical 1 and logical 0) is received at the output of transistor-based circuit.

The fragment of typical combinational circuit example *c17_i89* used in international scientific practice was selected for analysis of all-level faults of combinational circuits. The scheme of this circuit is presented in Fig. 1.

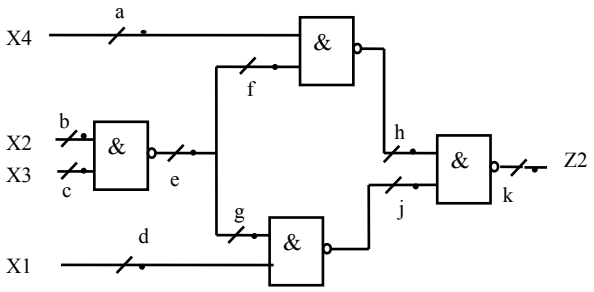

Fig. 1. Logical scheme of example *c17_i89* fragment: letters mark the paths in which faults of logical unit and logical zero (•) are simulated

Electrical circuit diagram of typical combinational scheme example *c17_i89* fragment was developed for physical fault analysis. CMOS and ESL logic was selected for transistor-based implementation of logical scheme, because circuits of these types are most common at the present time. Implementations of transistor-based logical scheme were designed according to the logical function performed by the example and they are not the sum of logical element circuits.

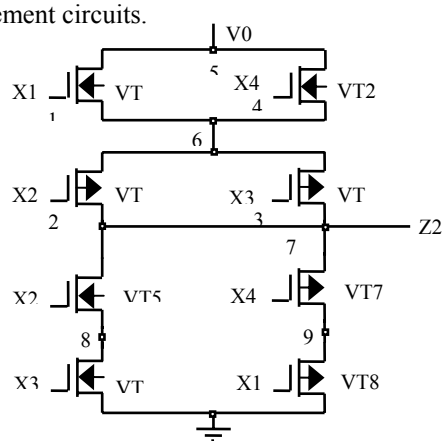

Fig. 2. Electric circuit of example *c17_i89* fragment first implementation CMOS1

Transistor-based circuit was simulated using electronic circuit analysis software package PSPICE in order to analyze CMOS circuit faults and determine fault diagnostics possibilities. Schichmann and Chodges model was used to describe nMOS and pMOS transistors. Comprehensive description of simulation process is provided in [3]. Performance of functional (good) circuit and circuit with individual faults was simulated.

During analysis of CMOS circuits the following type of physical fault model was applied: a) closed transistor, b) open transistor, c) circuit nodes short-connected, d) discontinuities at the inputs.

Three implementations of the same logical function were created for wider analysis of fault range. CMOS logic and transistors connected in series were used for the first realization (Fig. 2), CMOS logic and transistors connected in parallel were used for the second (Fig. 3), ESL logic – for the third (Fig. 4). ESL circuits performing particular logical function can be represented by equivalent switch circuit similarly like CMOS circuits. On purpose to form simpler and more practical implementations of transistor-based circuit for physical fault analysis, the function performed by typical *c17_i89* example fragment was minimized and it assumed the following form: $Z_2 = \overline{X_2 X_3 + \overline{X_1 + X_4}}$ (first implementation) and $Z_2 = \overline{X_2 X_3 + \overline{X}_1 \overline{X}_4}$ (second and third implementation).

Beside the analysis of transistor faults the set of test vectors was formed to verify the function of the circuit and determine constant faults of the logical circuit.

Analysis of function faults and logical circuit constant faults was performed using simulation system CADENSE. During simulation of function faults of typical example *c17_i89* fragment it was found that six test series sets are required to verify these faults. 20 logical unit and logical zero faults in all circuit paths were imitated during simulation of logical circuit of typical example *c17_i89* fragment (Fig. 1). Four test series sets were required to check thoroughly these faults. Four test series sets were also required to check thoroughly the faults of modified logical circuit, but they consist of another group of tests. Formed tests for verification of circuit-performed function and determination of logical circuit constant faults were used to diagnose physical faults of transistor-based circuits.

46 faults were simulated in electric circuit of CMOS1 fragment, 8 of them are gate discontinuities; 8 – open transistors; 4 – input discontinuities; 26 – short connections.

64 faults were simulated in electric circuit of CMOS2 fragment, 10 of them are gate discontinuities; 10 – open transistors; 4 – input discontinuities; 40 – short connections. Fault investigation results are presented in Tables 1 and 2. During analysis of ESL fragment (Fig. 4) the following type of physical fault model was applied: a) logical unit at the transistor input (open transistor), b) logical zero at the transistor input (closed transistor), c) current source discontinuity, d) short connections of circuit nodes. In the circuit logical unit and logical zero faults are simulated at the transistor base node. In this case logical unit at the transistor input imitates short connection between emitter and collector, i.e. one fault; logical zero at the transistor input imitates emitter discontinuity, base discontinuity, collector discontinuity, short connection with power supply bys, i.e. four equivalent faults; if logical zero is present at the diode input, then emitter discontinuity, base discontinuity is imitated here, i.e. two equivalent faults; current source discontinuity imitates emitter discontinuity, base discontinuity, collector discontinuity, i.e. three equivalent faults. 109 faults were simulated in ESL circuit, 14 of them are logical unit at the transistor input; 14 – logical zero at the transistor input; 2 – current source discontinuity; 32 – short connections. Results of fault investigations are presented in Tables 1 and 2..

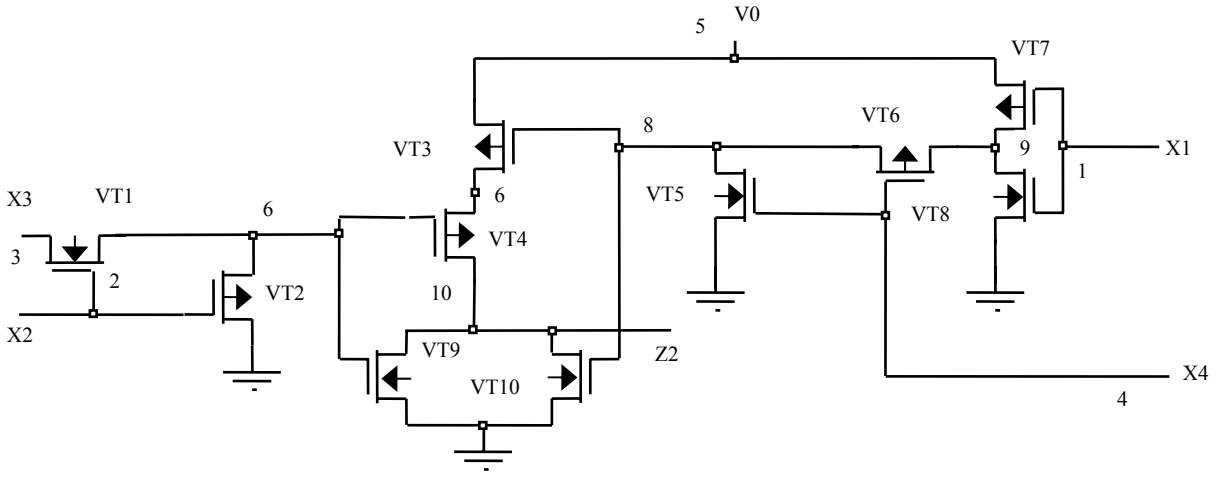

Fig. 3. Electric circuit of example *c17_i89* fragment second implementation CMOS2

Table 1. Comparison of verification of combinational circuit fragment performed function faults and transistor-based circuit faults

Circuit title	Number of simulated transistor faults	Number of non-determinable faults	All constant faults		Visi trumpųjų jungimų gedimai		Visi gedimai	
			Verifies	%	Verifies	%	Verifies	%
first implementation - CMOS1	46	1	19	100	26	100	45	100
second implementation- CMOS2	64	10	15	100	39	100	54	100
third implementation - ESL	109	14	76	100	19	100	95	100

Table 2. Comparison of verification of combinational circuit fragment logical scheme faults and all transistor-based circuit faults

Circuit title	Constant faults			Short circuit faults			All faults		
	Verifies	No	%	Verifies	No	%	Verifies	No	%
FIRST TEST SET									
first implementation - CMOS1	19	–	100	26	5	80,8	45	5	88,8
second implementation- CMOS2	15	3	80	39	11	71,8	54	14	74,1
third implementation - ESL	76	23	69,7	19	4	78,9	95	27	71,6
SECOND TEST SET									
first implementation - CMOS1	19	–	100	26	10	61,5	45	10	77,8
second implementation- CMOS2	15	6	60	39	11	71,8	54	17	68,5
third implementation - ESL	76	17	77,6	19	4	78,9	95	21	77,9

Investigation results

Variants of physical fault diagnostics presented in Table 1 reflect the situation, when physical faults at the transistor level are verified by tests used to determine circuit performed function faults.

Comparison of verification possibilities of combinational circuit fragment logical and transistor-based circuit faults is presented in Table 2. First test variant of example *c17_i89* fragment for logical circuit is distinguished and second test variant for modified logical circuit of the same fragment, formed according transistor implementations, is distinguished.

It is investigated, by what degree tests for verification of faults of separate fragment logical circuit are suitable to determine physical (transistor level) faults of these circuits. Their suitability to diagnose transistor-based circuit constant faults, short connections and all faults simulated in the circuit is analyzed separately.

The group of constant faults includes the following faults: closed transistor (gate discontinuity), open transistor, input discontinuity. Indeterminate (X) constant failures and indeterminate short connections form quite a large group of faults, when due to fault at the output of transistor-based circuit intermediate signal (between logical 1 and logical 0 levels) is received. We make an assumption at this work, that faults of this group are also verified.

Conclusions

1. A larger set of test series is required to verify the function performed by investigated combinational circuit fragments than to verify constant faults of the logical circuit.
2. Investigations show, that function tests of analyzed combinational circuits are suitable to detect almost all physical faults of transistor-based circuit (both for constant faults and short connections), at the same time logical circuit constant fault verification tests are not suitable to determine all faults.
3. There can be several implementations of transistor-based circuit and they are formed according to logical function mostly. Thus, in order to discuss how logical gate circuit tests are suitable to determine physical faults of transistor-based circuits, the former should be related to particular transistor-based implementation.

References

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3. **Benisevičiūtė R., Jusas V., Šeinauskas R**. Dinaminių KMOP trigerių diagnostikos ypatumai // Elektronika ir elektrotechnika. – Kaunas: Technologija, 1996. – Nr.5. – P. 26–28.
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R. Benisevičiūtė. Specific Features of Faults of Combinational CMOS Circuits // Electronics and Electrical Engineering. – Kaunas: Technologija, 2006. – No. 6(70). – P. 83–86.

This research work investigated a problem of application of transistors level fault model and its adequacy to faults at logical level of circuit. There were elaborated the faults at logical and at functional level using the software package CADENCE. The faults at transistors level were simulated by software package PSPICE. There were done the comparative results of fault simulation and fault coverage at transistors level and at logical level of CMOS circuit. Ill. 3, bibl. 4 (in English; summaries in English, Russian and Lithuanian,).

Р. Бенисявичюте. Особенности диагностики дефектов комбинаций КМОП схем // Электроника и электротехника. – Каунас: Технология, 2006. – № 6(70). – С. 83–86.

Анализируется возможность применить модель физических неисправностей транзисторов КМОП схемы, ее адекватности логическим схемам неисправности. Рассмотрены неисправности функции и логической схемы данных примеров при помощи их моделирования системой CADENCE. Также представлены результаты анализа физических неисправностей транзисторов, моделируя их пакетом анализа электронных схем PSPICE. Представлены сравнительные результаты анализов. Ил. 3, библ. 4 (на английском языке; рефераты на английском, русском и литовском яз.).

R. Benisevičiūtė. KMOP kombinacijų schemų gedimų diagnostikos ypatumai // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2006. – Nr. 6(70). – P. 83–86.

Išanalizuotos galimybės taikyti KMOP schemos tranzistorių fizinių gedimų modelį, jo adekvatumas loginės schemos gedimams. Nagrinėti tiriamų pavyzdžių funkcijos ir loginės schemos gedimai, modeliuojant juos CADENCE sistema. Nagrinėti tiriamų pavyzdžių tranzistorių fiziniai gedimai, modeliuojant juos elektroninių schemų analizės programų paketu PSPICE. Pateikti lyginamieji KMOP schemos tranzistorių fizinių gedimų nustatymo schemos funkciją tikrinančiais ir loginės schemos gedimus lokalizuojančiais testų sekų rinkiniais rezultatai. Il. 3, bibl. 4 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).