Research of Features of Synthesizer for High Speed Communication Systems

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Introduction

High speed is the main feature of the modern communications. The number of users as well as the range of data and complexity of networks are correlated. In many kinds of equipment, it is important to produce and readily control accurate waveforms of various frequencies and profiles. Many applications in electronics today involve gathering and decoding data for digital signal processing, analog measurements, fiber optics, and high-frequency communications. Synthesizer adoption practice can give the analysis and tools for engineer who needs to bring new technology products and services to market successfully. Engineers should analyze the synthesizer's adoptions S-curve and the demands of communication systems. The statistical analysis of synthesizer's parameters and communications systems is effective method.

Today faster, smarter radio frequency (RF) synthesis systems are enabled by introducing the industry's first low cost, low power, monolithic solution to integrate both direct digital synthesis (DDS) and phased locked loop (PLL) circuitry [1-3].

The main point of the article is to evaluate what advantages the connection of two different technologies provide: PLL and DDS.

The tasks: 1) Analysis of synthesizer parameters and advantages; 2) To analyze which parameters are most important for these devices using statistical research.

Features of the solution for connection of PLL and DDS

Digital technology continues to replace many analog functions in modern system architectures [4]. One of the latest contributors to this trend is the AD9956. The device is comprised of DDS and PLL circuitry. The best features of those two technologies are connected [1-2]. Important applications exist in communications systems that require agile frequency sources with low phase noise and spurs, combining - as DDS does - excellent frequency-tuning resolution and spectral performance [1,5-6].

Features and advantages: The AD9956 is Analog Devices newest Agile RF synthesizer. The DDS features a 14-bit DAC operating at up to 400 MSPS and a 48-bit frequency tuning word (FTW). The PLL circuitry includes a phase frequency detector with scaleable 200 MHz inputs (divider inputs operate up to 655 MHz) and digital control over the charge pump current. The device also includes a 655 MHz CML-mode PECL-compliant driver with programmable slew rates. The AD9956 uses advanced DDS technology, an internal high speed, high performance DAC, and an advanced phase frequency detector/charge pump combination, which, when used with an external VCO, enables the synthesis of digitally programmable, frequency-agile analog output sinusoidal wave forms up to 2.7 GHz. The AD9956 is designed to provide fast frequency hopping and fine tuning resolution (48-bit frequency tuning word). Information is loaded into the AD9956 via a serial I/O port that has a device write-speed of 25 Mb/s. The AD9956 DDS block also supports a user-defined linear sweep mode of operation. The AD9956 is specified to operate over the extended automotive range of -40 °C to +125 °C [1].

Typical application circuits

The AD9956 includes an RF divider (divide-by-R), a phase frequency detector, and a programmable output current charge pump. Incorporating these blocks together, engineer can generate many useful circuits for frequency synthesis [1]. There are presented five application circuit explanations:

1) Dual-Clock Configuration;
2) Fractional-Divider Loop;
3) LO and Baseband Modulation Generation;
4) Optical Networking Clock;
5) Direct Upconversion.

In loop (Fig. 1), M =1, N =16, and R =4. The DDS tuning word is also equal to ¼ so that the frequency of CLOCK1' equals the frequency of CLOCK1. Phase

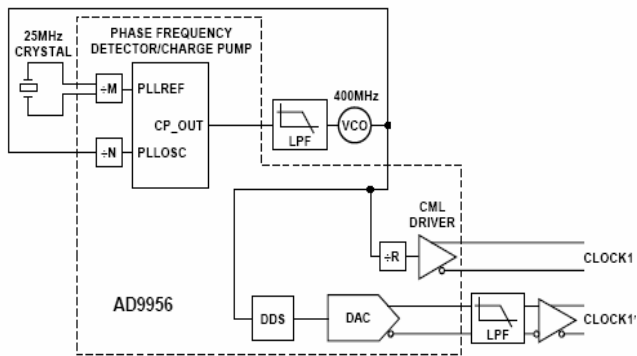adjustments in the DDS provide a 14-bit programmable rising edge skew capability of CLOCK1' with respect to CLOCK1.

Fig. 1. Dual-clock configuration

This loop (Fig. 2) offers the precise frequency division (48-bit) of the DDS in the feedback path as well as the frequency sweeping capability of the DDS. Programming the DDS to sweep from 24 MHz to 25 MHz sweeps the output of the VCO from 2.7 GHz to 2.6 GHz. The reference in this case is a simple crystal.
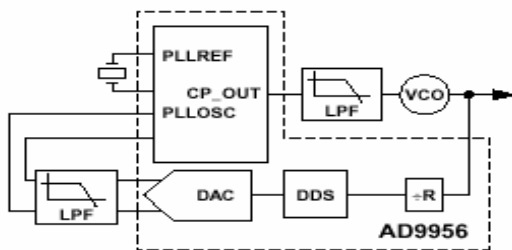

Fig. 2. Fractional - divider loop

Using the AD9956 's PLL section to generate (Fig. 3) an local oscillator (LO) and the DDS portion to generate a modulated baseband, this circuit uses an external mixer to perform some simple modulation at RF frequencies.
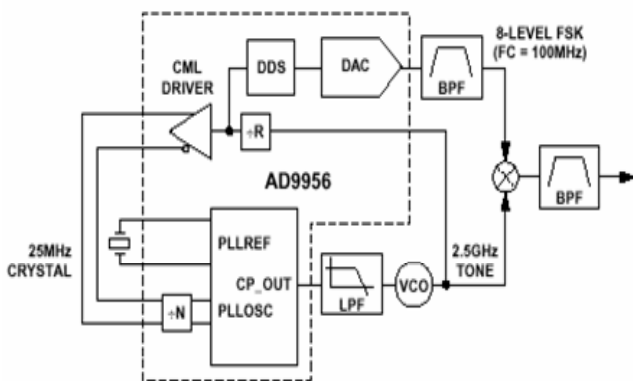

Fig. 3. LO and Baseband Modulation Generation

AD9956 can be configured as an optical networking clock (Fig. 4). The loop can be used to generate a 622 MHz clock for OC12 Fiber Converters. The DDS can be programmed to output 8 kHz to serve as a base reference for other circuits in the subsystem.
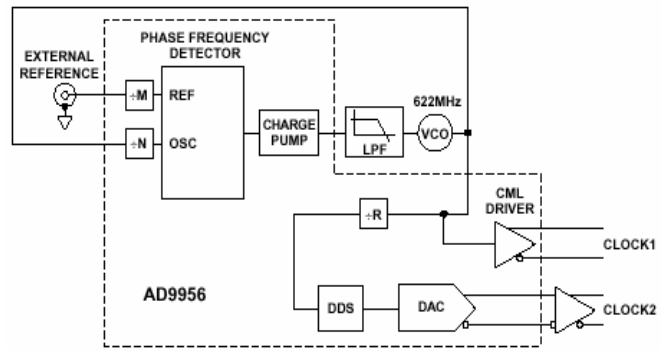

Fig.4. Optical Networking Clock

The AD9956 is configured (Fig. 5) to use the DDS as a precision reference to the PLL. Since the VCO is <655 MHz, it can be fed straight into the phase frequency detector feedback input (with the divider enabled) [1].
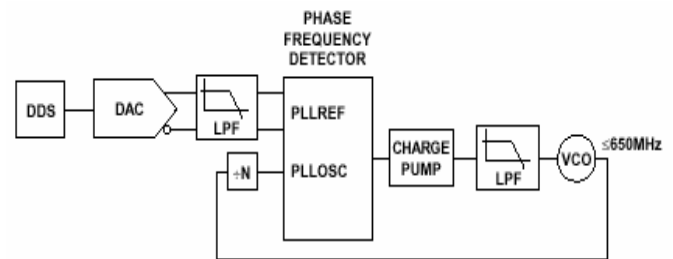

Fig. 5. Direct upconversion

PLL technology advantages to synthesizers

Even though DDS technology offers excellent frequency and phase tuning characteristics, upconversion is required to take advantage of these features at UHF (ultra high frequency) or microwave frequencies where PLL is preferable [7-8].

DDS designs often end up involving numerous components and hence are not suitable for monolithic RF transceivers. This is one of the main reasons why the PLL (indirect synthesizer) became the dominant architecture for frequency synthesis [4].

A frequency synthesizer allows the designer to generate a variety of output frequencies as multiples of a single reference frequency. The main application is in generating local oscillator signals for the up and down conversion of RF signals [3].

The primary advantage of a PLL based clock synthesizer is low cost [3].

DDS technology advantages to synthesizers

Direct-digital-synthesis (DDS)-based synthesizers are primarily known as agile frequency sources with low phase noise and excellent spurious performance. In many applications, they offer significant advantages over phase-locked-loop (PLL) synthesis methods like sub-hertz frequency tuning resolution, phase offset and output amplitude control. By using a hybrid solution (AD9956), the tuning resolution of the DDS can enhance the tunability of the overall system to a level not possible with a PLL alone [3, 7-9].

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The output phase noise of a DDS synthesizer is actually better than that of its reference clock source, while analog PLL-based synthesizers have the disadvantage of actually multiplying the phase noise present in their frequency reference [2].

So advantage of DDS is that the frequency of the output signal can be as accurate as the crystal controlled oscillator used as a reference signal to the communications system. Another advantage of DDS is related to the first: a DDS can generate frequencies with very high precision. The digital circuitry of a DDS signal can have as much frequency precision as the digital circuitry implements. If the DDS circuit has a 48-bit counter, it can offer up to 48 bits of frequency resolution [5].

Advantage of DDS is that the engineer may reproduce virtually any waveform if it has RAM waveform storage. The DDS operates by "playing back" a waveform stored in its memory. Typically, a Sine, Square, Triangle and similar waveforms are built into every function generator [5-6].

Statistical research of DDS and PLL parameters

DDS parameters

Analog Devices presents the most important DDS parameters (Table 1) that are explained below:

Output Compliance. The output compliance refers to the maximum voltage that can be generated at the output of the DAC to meet the specifications. When voltages greater than those specified for the output compliance are generated, the synthesizer may not meet the specifications listed in the data sheet.

Digital Clock Input (Master fclk). DDS output frequencies are expressed as a binary fraction of the frequency of Master fclk. This clock determines the output frequency accuracy and phase noise.

Signal to noise (Noise + Distortion). Signal to noise (Noise + Distortion) is measured signal to noise at the output of the DAC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the non-fundamental signals up to half the sampling frequency (Master fclk /2) but excluding the dc component. Signal to noise (Noise + Distortion) is dependent on the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical Signal to noise (Noise + Distortion) ratio for a sine wave input is given by *Signal to noise (Noise + Distortio*n) = (6.02 *N* + 1.76) *dB* where *N* is the number of bits. Thus, for an ideal 10-bit converter, Signal to noise (Noise + Distortion) = 61.96 dB.

Full-Scale adjust control (FS). A resistor (R_{SET}) is connected between this pin and analog ground (AGND). This determines the magnitude of the full-scale DAC current.

Resolution. The output phase of the DDS is typically controllable with 10-bit to 14-bit resolution, giving programmable phase resolution to <0.1 degrees. This high resolution means that the function generator is able to exactly generate a desired output frequency and it also means that the generator can make very precise changes in frequency.

Tuning Word With. The DDS, with its high tuning word, allows the reference frequency to be very narrowly tuned, resulting in fine adjustment of the output frequency much more conveniently than through the use of a fractional-N PLL [1, 5-6].

DDS Statistical research

After analysis of main parameters of synthesizers we will use a linear model of regression and will find out: 1) what parameters in the manufacturing are most important for these devices; 2) correlation of parameters.

The data for research is taken from Analog Device specifications [1]. The accuracy of the results depends from number of synthesizers and rationality of selection [10]. For the DDS case we will have 20 synthesizers. In the article the correlation of main DDS parameters and other statistical coefficients is calculated. The correlations between parameters are meaningful if the correlation coefficient exceeds 50% [11-12].

The linear equation of regression has an expression:

$$y = b_0 + b_1 x_1 + b_2 x_2 + b_3 x_3 + b_4 x_4 + b_5 x_5 + b_6 x_6 + \ldots + b_n x_n + m. \quad (1)$$

In the formula (1) y-value is a function of the independent x-values. The b-values are coefficients corresponding to each x-value, and m is a constant value [11-12].

The bolded numbers in the Table 1 mean that correlations between parameters are strong (with reliability $\alpha = 0,05$). The research will let to establish connection between improvement of synthesizers and prices using regression model with „Excel" program. In this analysis we determine what influence on the price is done when parameters of synthesizer are improved [10].

The prices of synthesizers depend on quality of most important parameters (Table 1) that is represented in Analog Device specifications [1].

The data of statistical research shows that very important parameter for the synthesizers manufacturing is the maximum allowable input frequency, because it determines output frequency accuracy and phase noise. Bigger input frequency reduces the number of operation and thereby the lower phase noise and bigger accuracy is achieved. When Master fckl frequency increases the price of synthesizers rises up because the investments on development increase cost of manufacturing (Fig. 6). The coefficient of linear regression shows that frequency of master clock improvement has big influence on DDS price, because the coefficient of regression is very high (89,3 %) (Table 1). Besides frequency of master clock increment of such parameters was determined like I supply, full-scale (FS) DAC current, compliance range. If frequency increases, that will demand a bigger current consumption and compliance range.

Table 1. Correlation of DDS parameters

	Master fclk	Resolution (Bits)	Tuning Word Width (bits)	I Supply total (max), mA	FS I_{out} (mA nom)	Compliance Range (V)	Noise level, dB (MHz = ~Mfclk/3,)	Price, EUR
Master fclk	1	30,52%	21,18%	43,56%	**65,28%**	**90,21%**	-18,49%	**89,30%**
Resolution (Bits)		1	40,85%	**97,83%**	-9,62%	23,59%	32,60%	8,51%
Tuning Word Width (bits)			1	**94,19%**	18,19%	3,40%	5,86%	18,68%
I Supply total (max), mA				1	33,07%	-14,68%	-9,50%	**81,10%**
FS Iout (mA nom)					1	**58,03%**	11,41%	**64,15%**
Compliance Range (V)						1	-2,56%	**80,43%**
Noise level, dB							1	19,93%
Price, EUR								1

The maximum allowable consumption of current (I supply) is very sensitive to the changes of other parameters (master fclk 43,56%; resolution 97,83%; tuning word width 94,19%) and it determines the price of synthesizers very strongly (81,1%). Such parameters like resolution, tuning word width, and noise level don't correlate with price because the diffusion of them is not big and impact is not direct. They impact the price indirectly and commonly over the factors like fast switching action, fast settling time and etc.
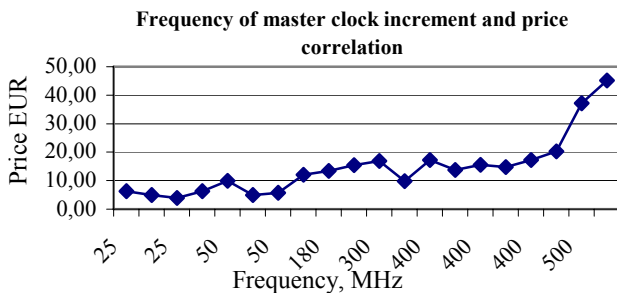
Fig. 6. Master clock frequency increment and price correlation

The multiple coefficients of linear regression show (92,3%) (Table 2) that analyzed parameters require particularly high quality and level because they are most important for DDS when they are integrated with the communication systems. That proves the correlation between parameters and price that is coming from the demands of communication systems.

The coefficient of determination (R square= 85,1%) shows how strongly concrete improvement (modification) of synthesizer raise up the price of all system.

Table 2. DDS Multiple regression statistics

| Multiple R	0,923
R Square	0,851
Adjusted R Square	0,783
Standard Error	4,845

PLL parameters

Analog Devices presents the most important PLL parameters (Table 4) that are explained forward:

Radio reference frequency: A good, high quality, low-phase-noise reference is crucial to a stable low-phase-noise RF output. A square wave or clipped sine wave available from a TCXO crystal offers excellent performance, because the sharper clocking edge results in less phase jitter at the R-counter output. The AD9956 family features on-board oscillator circuitry allowing low cost AT-cut crystals to be used as the reference. While predictable AT crystals cost one third as much as TCXOs, their temperature stability is poor unless a compensation scheme with a varactor is implemented.

Reference input frequency (Max REF_{in}). This is a CMOS input with a nominal threshold of VDD/2 and a dc equivalent input resistance of 100 kΩ (Fig. 7). This input can be driven from a TTL or CMOS crystal oscillator or it can be ac-coupled.
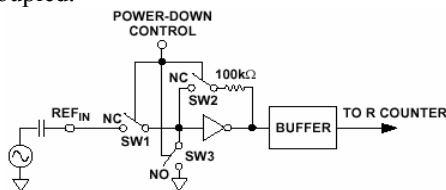
Fig. 7. Reference Input Stage

Phase noise is probably the most crucial specification in PLL selection. In a transmit chain, the linear power amplifier (PA) is the most difficult block to design. A low-phase-noise LO will give the designer greater margin for non-linearity in the PA by reducing the phase error in the up-conversion of the baseband signal. The system maximum phase error specification for GSM receivers/transmitters (Rx/Tx) is 5° rms. In order to demodulate the desired RF signal, either the transmit side will require higher output power, or the LO phase noise will need to be improved [1, 5, 8].

PLL statistical research

For the PLL case we will have 18 synthesizers [1]. In the article the correlation between main PLL parameters and other statistical coefficients is calculated.

The data of statistical research shows (Table 4) that parameters weakly correlate with a price, because the coefficients of correlations do not exceed 50%. So the changes of parameters are not supple, because the prices of communication systems don't change signally. PLL technology is cheaper than DDS, because it has more advantages. The price's diffusion to complex of different

parameters isn't big; consequently the improvement by market demands does not raise the price up.

The multiple coefficient of linear regression prove out (66,2%) that analyzed parameters don't have strong correlation to the system price (Table 3). Also coefficient of determination (R square= 43,8%) shows that improvement of synthesizers do not raise up the system price meaningly.

Table 3. PLL Multiple regression statistics

Multiple R	0,662
R Square	0,438
Adjusted R Square	0,251
Standard Error	1,319

However PLL parameters correlate between themselves much closely than parameters of DDS technology. That shows that elements of PLL circuitry are strongly dependent from each other.

The coefficient of linear regression shows that almost all parameters of PLL technology have correlation between itself (Table 4). The strongest correlation is between supply current and reference input frequency (90,1%), radio frequency input (85,11%) (Fig. 8).
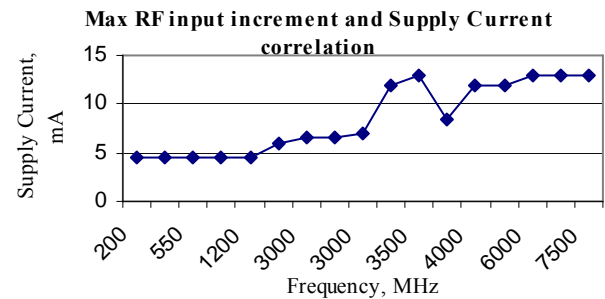
Fig. 8. RF input increment and supply current correlation

**Table 4.** Correlation of DDS parameters

	Max RF Input MHz	Norm Phase Noise dBc/Hz	Max REFin MHz	Supply Current mA	Price EUR
Max RF Input MHz	1	**-75,05%**	**72,90%**	**85,11%**	7,61%
Norm Phase Noise dBc/Hz		1	-44,10%	-49,82%	-11,21%
Max REFin MHz			1	**90,18%**	44,92%
Supply Current mA				1	43,02%
Price EUR					1

Synthesizer's development and adoption curves

Synthesizer Adoption Practice (SAP) can give the analysis and tools for engineer who needs to bring new technology products and services to market successfully. It's important to know where your current and future customers are located on the technology adoption S-curve (Fig. 9) [13]. The functional dependences charted in the research are just as S-curve (Fig. 8, 9). It proves that curve falls down when the demand of better parameters in the communication systems emerges. Then the engineers of Analog Device analyze new demands or requirements for synthesizers and make decision how to improve devices and the curve begins to arise again (Fig. 9).

Communication system planners should assess the relative impact of a technology and act early for high-impact technologies, no matter what is their normal level of technology aggression, while waiting for others to move first on technologies that are less relevant to the core of their system [13].
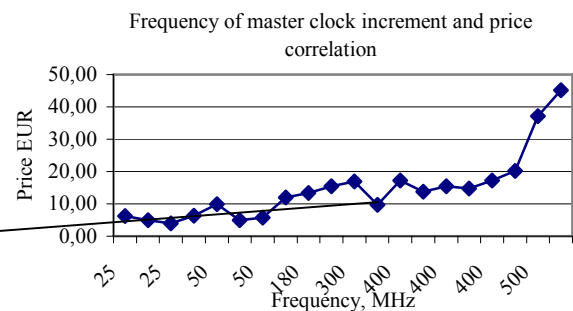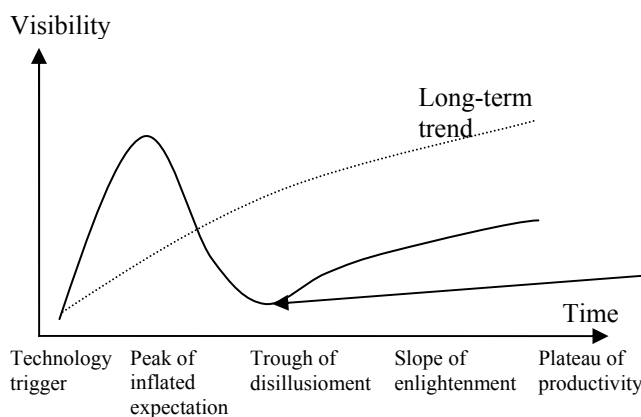
Fig. 9. Synthesizer's development and adoption curves

Conclusion

However, now that both PLL and DDS circuits are available as low-cost components, it is becoming practical to consider designing a hybrid circuit combining both techniques, thus eliminating the trade-offs. The designer can take advantage of both methods to obtain an overall solution that outperforms individual PLL or DDS designs. In this article such advantages of combining both techniques were identified: fine frequency resolution; fast

switching action; fast settling time; wide bandwidth; very low power; low phase noise and spurious noise.

The statistical research shows that concrete improvement (modification) of DDS synthesizer parameters raise up the price of all communication systems (R square= 85,1%). Situation is converse with PLL technology where price's is not wide-ranging and don't supple. It determines why PLL-based clock synthesizer is low and stabilized cost.

The functional dependences charted in the research are just as S – curve. It proves that curve falls down when the demand of better parameters in the communication systems emerges. Engineers should analyze the synthesizer's adoptions S-curve and the demands of communication systems.

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J. Sveikata, R. Morkvėnas. Research of Features of Synthesizer for High Speed Communication Systems // Electronics and Electrical Engineering. – Kaunas: Technologija, 2006. – No. 3(67). – P. 71–76.
There are analyzed two different technologies - PLL/DDS frequency synthesizers. DDS providing a fine-tunable reference for a PLL technology, and a PLL that gives the better spectrum of DDS signal output.
Article presents parameters of synthesizers, and i typical application circuits are shown. Also it was proven that parameters are most important for signal source. For that purpose a statistical research is used revealing a dependence between synthesizer's parameters improvement and its prices. The statistical research uses a regression model in Excel software environment. The functional dependences between varied parameters are relevant when analyzing technology of synthesizers and its development. The results of a research and presented graphs predict the practice of synthesizer adoption where adoption of technology S-curve tendency is obvious. Ill. 9, bibl. 13 (in English; summaries in English, Russian and Lithuanian,).

Ю. Свейката, Р. Морквенас. Исследование синтезатора для высокоскоростных систем связи // Электроника и электротехника. – Каунас: Технология, 2006. – № 3(67). – С. 71–76.
Анализированы гибридные синтезаторы частот на основе двух технологий: DDS, обеспечивающей удобную регулировку частоты, и PLL, обеспечивающей относительно высокую спектральную чистоту.
Представлены функциональные схемы для типичных применений Analog Devices синтезаторов.Показаны преимущества синтезатора новой технологии. При помощи статистического исследования оценено влияние параметров на цену синтезатора. По результатам исследования подтверждается развитие технологии синтезаторов по кривой S вида. Ил. 9, библ. 13 (на английском языке; рефераты на английском, русском и литовском,).

J. Sveikata, R. Morkvėnas. Didelio greičio ryšio sistemų sintezatorių tyrimas // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2006. – Nr. 3(67). – P. 71–76.
Analizuojami dviejų skirtingų technologijų – PLL ir DDS dažnių sintezatoriai. Juose DDS suteikia puikias valdymo charakteristikas PLL technologijai, o PLL technologija gerina DDS išėjimo signalo spektrą.
Tiriami nagrinėjamų sintezatorių parametrai, pateikiamos tipinės sintezatorių naudojimo struktūros. Parodoma, kurie parametrai yra svarbiausi šiems signalų šaltinims. Tam naudojamas statistinis tyrimas, atskleidžiantis priklausomybę tarp sintezatoriaus parametrų tobulinimo ir jo kainos. Statistiniems tyrimams naudojami regresijos modeliai Excel programinėje terpėje. Pateikiamos funkcinės priklausomybės tarp įvairių parametrų yra aktualios analizuojant sintezatorių technologijų bei jų rinkos plėtrą. Tyrimo rezultatais ir pateiktais grafikais patvirtinama sintezatorių įvaldymo praktika, kurioje akivaizdi technologijos įsisavinimo s kreivės tendencija. Il. 9, bibl. 13 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).