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Design adaptation of an electronically tunable oscillator using a low performance linearized CMOS operational transconductance amplifier

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ABSTRACT

This paper presents the implementation of commercially available CMOS devices with unfavorable properties, such as low output resistance, in an application designed to mitigate these limitations. By employing a specific topology and considering key design parameters, the proposed approach minimizes the adverse effects of low output resistance. This design focuses on a linearized operational transconductance amplifier (OTA) based on CMOS transistors, featuring with very low output resistance. This OTA is further integrated into an LC oscillator, where the associated disadvantages are suppressed through a specialized topology and careful selection of parameter values that are unaffected by the low OTA output resistance. The operational verification targets a frequency range of several hundred kHz and a linearly processed voltage range of several hundred mV. The linearized OTA-based low-gain amplifier/attenuator offers a linearity error within −7% (±500 mV). The proposed OTA implementation in the oscillator introduces highly simplified method for adjusting the oscillation condition using a single grounded element while minimizing the adverse effects of low output resistance of OTA. Additionally, the tunability of the oscillator using varactor diodes achieving a range from 120 kHz to 273 kHz for a voltage varying from 0 V to 5 V.

1. Introduction

Modern discrete and integrated analog circuit design faces numerous challenges due to the performance limitations of active devices. These limitations are due to the decreasing supply voltage levels and the continuous miniaturization of fundamental components, such as MOS transistors, in advanced fabrication processes. Similar constraints also affect typical many commercially available active devices intended for custom designs. Circuit designers have no direct control over the performance of these pre-fabricated components and must adapt their designs to the available device characteristics. In many cases, improving these performance limitations at the chip design stage is not feasible. Therefore, it is essential to explore methods for achieving accurate circuit design (regarding comparison with theoretical expectations) even when working with devices that have less than ideal performance compared to those of previous decades (larger CMOS processes).

Indicated issues are practical consequences of implementation of various commonly used active devices [1,2] in the design, which significantly affect key parameters of circuit application. This issue is particularly evident in active filter design [3–7], where the poor performance of active devices, such as low output resistance and limited DC gain, improperly influences the overall frequency response. These shortcomings lead to finite attenuation in stop bands (as demonstrated in recent works [5–7]) and cause deviations from theoretical expectations. The effects of finite resistance at circuit nodes where active devices are employed have been analyzed in detail in [3] and [4]. Such limitations are typical in modern fabrication technologies and become more significant as power supply and transistor channel lengths decrease [8]. In particular, the drain-source resistance can be significantly reduced, often reaching only a few tens of kΩ or even lower. However, modern fabrication processes and limited supply voltage constraints do not provide ideal device characteristics, nor do they allow for straightforward adaptation.

Based on extensive experience in the field of integrated analog circuit design, several approaches can be taken to address these limitations:

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a) Enhancing active device design at the fabrication stage (e.g., mirror cascoding [8] to improve output impedance, though this is often infeasible due to required structural modifications).
b) Modifying the circuit application (e.g., selecting a topology with certain immunity to undesirable characteristics or adapting the design to mitigate limitations),
c) Accounting for parasitic effects in the design specifications and ensuring their impact remains negligible (not always possible).

This paper focuses on approaches b) and c) simultaneously. The selected example uses commercially available devices that do not allow modifications to their intrinsic characteristics.

The design presented in this work is based on commercially available MOS transistors with low output resistance. We have the following question. Can we still achieve precisely operating systems using devices with such limitations? The existence of multiple solutions to the same problem provides valuable insights – various circuit topologies based on similar principles can still meet the required performance criteria. The results presented in this paper demonstrate that even devices with non-optimal characteristics can be effectively utilized (the harmonic LC oscillator chosen as an example in this paper) if specific design strategies, solutions, and topologies are employed to address their limitations. More specifically, we demonstrate the design of an oscillator circuit using an operational transconductance amplifier (OTA), similar to many recent works, but with very poor output resistance performance. Despite this limitation, the proposed design achieves precise and accurate operation, comparable to solutions that are not affected by such low-performance active devices. Our approach is based on points b) and c) outlined earlier: modifying the topology appropriately and considering for expected parasitic behavior during the design. As a result, these parasitic effects do not degrade the behavior of the circuit, and the ideal design equations closely match the practical results obtained.

The organization of the paper is as follows. Section 2 outlines the main motivation behind the proposed approach. Section 3 explains the design and characteristics of the linearized active element used in further sections. Section 4 presents the design and experimental verification of the targeted LC oscillator. Section 5 compares the key features of the oscillator with recent state-of-the-art solutions. Finally, Section 6 summarizes the main findings and conclusions of this work.

2. The idea explanation and motivation

The considered situation is illustrated in Fig. 1, where two types of oscillators utilizing operational transconductance amplifier(s) (OTAs) [1,2] are presented. The first type, shown in Fig. 1**(a)**, consists of two OTAs [9,10] with transconductances g_m, two capacitors, a resistor R_p and a negative resistor R_n, which is required to satisfy the oscillation condition. The circuit also includes the output resistances of the OTAs (R_{o1}, R_{o2}), which represent the most significant real features in this example of application. When both output resistances are low (on the order of a few kΩ), they significantly affect both the oscillation frequency and the oscillation condition, rendering standard design formulas [9,10] invalid. Consequently, the chosen values of R_p and R_n must be kept very low (tens to a few hundreds of Ω), while the capacitor values $C_{1,2}$ must be very large for low-frequency operation (kHz range). This approach is impractical because it increases power consumption and limits the available output currents of the OTAs, thereby limiting the output signal levels.

When the output resistances $R_{o1,2}$ ($R_{o1} = R_{o2} = R_o$) are very small, the oscillator configuration using only two capacitors and two OTAs becomes infeasible due to the excessive influence of parasitic parameters on both the oscillation condition and frequency. However, a simple modification of the topology – switching the capacitor-based structure in Fig. 1**(a)** to an LC-based configuration [11] – results in a significant improvement in mitigating the effects of the OTA output resistance. While coils are traditionally impractical for low-frequency applications due to their bulk and weight, modern implementations provide feasible solutions within the targeted frequency range [12]. Therefore, the most known solution in Fig. 1**(a)** depends primarily on the value of the OTAs output resistance, as it directly influences the circuit's performance and feasibility. In other words, changing the topology from the synthetic inductor-based solution (see Fig. 1**(a)**) to the LC-tank-based solution (see Fig. 1**(b)**) represents the implementation of point b). This change brings a beneficial interconnection in which the parasitic output resistance R_o appears as part of the LC tank losses. Consequently, R_o has a negligible impact on the oscillation frequency. In fact, in this case, R_o can be advantageous (as per point c)), because it reduces the influence of the OTA transconductance g_m on the oscillation condition. With proper selection of the parallel passive resistor value, R_o even enables simple implementation of an amplitude stabilization circuit, as discussed later. Furthermore, in the specific design, a low R_o value is actually beneficial, since the parallel resistor controlling the oscillation can be of a comparable value. For standard OTA-based oscillators, such as the topology in Fig. 1**(a)**, an acceptable value of R_o would need to be in the high tens or hundreds of kΩ (the larger, the better, ideally infinite). On the other hand, in the proposed Fig. 1**(b)**, a R_o of only a few hundred of Ohms to a few kΩ (easily available in practice and even compatible with optocouplers fulfilling condition $R \geq R_o$) remains sufficient to maintain stable oscillation without affecting the frequency. However, in standard topologies (Fig. 1**(a)**), such low R_o values would highly influence both

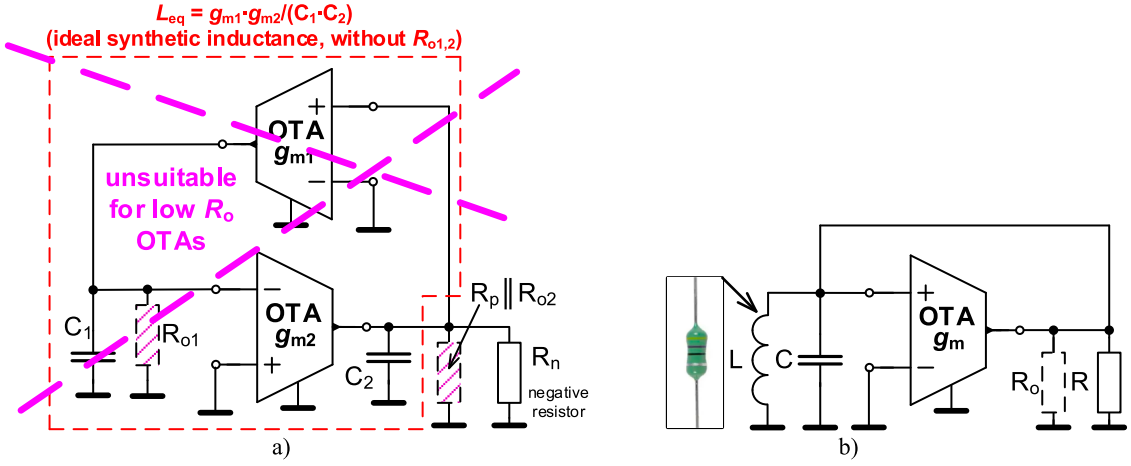


Fig. 1. Discussion of the oscillator solutions influenced by low output resistance of OTA: a) standard synthetic inductor-based solution using only capacitors as accumulation elements [9], b) LC type.

the oscillation and the oscillation condition.

The key advantage of the solution shown in Fig. 1**(b)** is that the output resistance R_o is concentrated at the same node as the LC tank. In fact, this means that R_o contributes only to the overall parallel losses of the circuit. Unfortunately, when R_o is very small, the OTA must compensate for these losses by providing a high transconductance (g_m), which is proportional to $1/R_o$. In practical implementations, achieving such a high g_m is often not feasible. Despite this limitation, the LC-based topology is still more suitable and mitigating the effects of low R_o compared to the capacitor-based topology in Fig. 1**(a)**. Now, only the LC tank (Fig. 1**(b)**) defines the intended electronic tunability instead of the parameters $g_{m1,2}$ (see Fig. 1**(a)**). The characteristic equation of this oscillator has the form of:

$$s^2 + \frac{(R + R_0 - g_m \cdot R \cdot R_0)}{R \cdot R_o \cdot C} s + \frac{1}{L \cdot C} = 0 \quad (1)$$

which gives the condition of oscillations in the form $R \geq R_o/(1 - g_m \cdot R_o)$. This condition is beneficial because has two consequences. If the R_o is very high, the oscillation condition simplifies to the standard form $R \geq 1/g_m$. If g_m is very small, the oscillation condition reduces to $R \geq R_o$. Thus, in both cases, the oscillation condition can be met independently of whether R_o is low or high. Additionally, this topology is particularly well-suited for OTAs with small, fixed g_m and linearization.

It is important to note – relevant to later sections – that the DC transfer response of a standard OTA employing either a bipolar or unipolar differential pair is highly nonlinear. Consequently, the generated waveforms maintain good spectral purity only for signal amplitudes up to a few tens of mV. The main advantages and disadvantages of both topologies are summarized in Table 1, which highlights the benefits of the topology shown in Fig. 1**(b)** for implementing active devices with low value of R_o.

The relation of issues indicated in Fig. 1**(a)** to typical applications (field of sine wave oscillator design using OTAs) are further discussed in Section 5 and referring to important works using OTAs or devices derived from the OTA principles. These solutions may suffer from imperfections in the OTA performance discussed in this work.

3. The active OTA using commercially available transistor fields

The nonlinearity of active devices is a significant issue for applications requiring linear operation, such as amplifiers, active filters, and harmonic oscillators. Standard OTAs are biased by a DC current source I_{bias}, which introduces significant nonlinearity in relationship between the differential input voltage and the output current. Specifically, for OTAs based on bipolar or unipolar devices, this relationship follows $I_o \sim \tanh(V_p - V_n)$ or $I_o \sim (V_p - V_n)\cdot(\text{constant} - (V_p - V_n)^2)^{1/2}$, respectively [13]. The DC bias current source allows to adjust the small-signal transconductance g_m of the differential pair end ensures a good common mode rejection ratio (CMRR) of the differential pair [8]. However, the dependence of g_m on I_{bias} has a nonlinear trend ($g_m \sim \sqrt{I_{bias}}$), and linearization of the differential pair is valid only for a fixed I_{bias} in the simplest cases. If a fixed g_m is acceptable and excellent CMRR is not required, the OTA design can be significantly simplified. In such cases, the bias current source can be simply omitted if there are no additional performance requirements, such as precise adjustment and excellent CMRR. The OTA design in Fig. 2 illustrates this simplified approach, where only four MOS transistors and two degeneration resistors R_S are sufficient to create a quite linear OTA using ALD1106/7 transistor fields [14,15].

Table 1
Comparison of both solutions shown in Fig. 1.

	Fig. 1(a)	Fig. 1(b)
Used type of OTA	Standard bias controlled g_m	Linearized fixed g_m
Type of electronic adjustment	Linear	nonlinear (range based on specific adjustment of LC tank)
Complexity	Higher	Low
Number of active elements	2 (3 including solution of negative resistor)	1
Number of external passive elements	3	3
Impact of OTA R_o (low value)	High	Insignificant
Generated levels	Tens of mV	Hundreds of mV
Accuracy of theoretical design equations (oscillation frequency) influenced by low R_o value	Low	High (independent on R_o)

The linearization of the OTA can be achieved in several ways [8,13]. The "active" methods address linearity issues by adding extra circuit elements, such as the cross-coupled quad configuration of a differential pair [13], or/and by applying reciprocal input–output transfer response. However, these techniques may affect AC performance and speed (frequency limitations), as they tend to increase the gate-source capacity [13]. In contrast, passive degeneration techniques [8] are effective for high-frequency amplifications, as they do not significantly increase the nodal capacitances in the transistor topology. However, the passive (degenerative) methods reduce the transconductance (g_m) compared with certain active methods or with solutions without degeneration. In such cases, the degenerative resistors (which can also be replaced by MOS element operating as a resistor) largely determine the overall g_m (and gain) of the differential pair. Nevertheless, the reduced g_m is not a significant issue in many cases (depending on gain requirements) when the improved linearity of the I-V response of the pair is more important than the nonlinear "quadrature law" behavior of the MOS g_m.

The degeneration itself does not intentionally affect the output resistance R_o. However, in topologies that use an additional resistor, the reduced bias current may increase R_o compared with a design without degeneration. The output resistance depends on the bias current in the output MOS transistors of the OTA (often the same as the bias current in differential pair or modified by current mirrors), i.e., $r_{ds} \approx 1/(\lambda \cdot I_{MOS/BIAS})$, where λ is the channel length modulation parameter, which also depends on the length of the element. In our design, the bias current in OTA topology is fixed (not adjustable), so the output branches have constant biasing, allowing us to select an optimal value to achieve a good performance between speed and significantly high value R_o. With a fixed bias current, R_o also remains fixed. In contrast, in standard bias-controlled OTAs (used for intentional g_m variation), the bias current is variable, which also causes R_o to vary (specific cases have specific range of R_o values). This can be mitigated by cascoding two sections, with the second OTA stage having fixed biasing. However, such an approach often increases both circuit complexity and power consumption. The requirements for high speed (which demand high bias currents for wide frequency bandwidth) and the high value of R_o are inherently in contradiction.

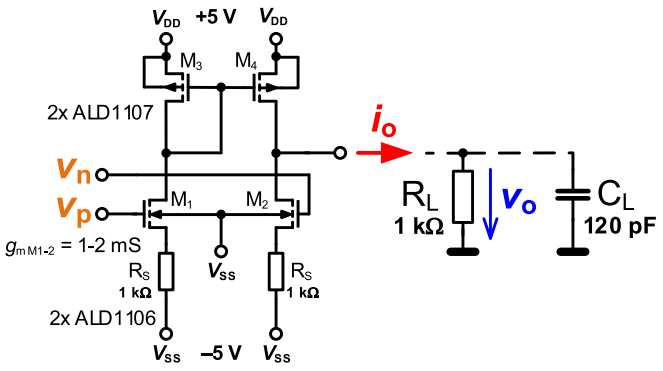


Fig. 2. Designed source degenerated OTA using available ALD1106/7 transistor arrays (four MOS transistors in total).

The ideal small-signal expression for the output current I_o is given by:

$$I_o = (V_p - V_n)\cdot GM = (V_p - V_n)\cdot \frac{1}{\left(\frac{1}{g_{m1,2}} + R_S\right)} \quad (2)$$

Based on (2), the source degeneration (R_S) has a significant effect on the overall transconductance *GM* (and the improved linearity) of the source degenerated differetial pair (Fig. 2), because the individual transconductances ($g_{m1,2}$) of MOS transistors ($M_{1,2}$) are quite low (approximately 1–2 mS) [14] when R_S selected in the hundreds of Ω. The output current of M_1 is directly copied into the output branch by a PMOS current mirror (acting as an active load) with $g_{m3,4} = 700$ μS and $r_{DS3,4} = 25$ kΩ [15], resulting in a high impedance output terminal. However, the output resistance $r_{DS1,2}$ of the NMOS transistors is relatively low (only 5 kΩ) [14], which complicates designs of specific applications, such as universal active filters [3–7]. Fortunately, specific design considerations and techniques can mitigate this disadvantage. When used as a linearized inverting or non-inverting voltage amplifier or attenuator (with $V_{in} = V_n$ and grounded V_p, or vice versa), the DC gain of the topology shown in Fig. 2 is given by:

$$K_{ampl0} = \frac{V_o}{V_{in}} \cong \pm\frac{R_L}{\left(\frac{1}{g_{m1,2}} + R_S\right)} \quad (3)$$

Fig. 3 illustrates the A-V responses and transconductance behavior of a standard (non-linearized) OTA. These auxiliary results serve as a reference for further comparisons with the designed amplifier/attenuator. The *GM* value was set to 0.5 mS, approximating the available transconductance of the linearized circuit in Fig. 2, where $g_{m1,2}$ was determined as 1 mS (based on [14]) and R_S was set to 1 kΩ.

The OTA design requirements are as follows: linear operating range between: ±0.5 V (linearity error up to ±10 %); frequency bandwidth $BW > 1$ MHz for a load of $R_L = 1$ kΩ and $C_L = 120$ pF. The large value of C_L (fulfilling *BW*) is significantly higher than the expected stray capacitances of the element terminals. The supply voltage is ±5 V and the total supply current is up to 7 mA (resulting in a power consumption of 70 mW). The DC transfer responses of the experimentally tested OTA, used as a voltage amplifier/attenuator ($|K_{ampl0}| = 0.5$), are shown in Fig. 4. The degenerated OTA shows a slightly lower gain than the ideal case but significantly improved linearity (linearity error of − 7 %) compared to the − 20 % error observed in a standard (non-degenerated) OTA. The output current reaches approximately ±250 μA within the given input range. The AC responses are shown in Fig. 5. The expected maximum DC gain is $A_0 \cong g_{m1,2}\cdot R_o \cong g_{m1,2}\cdot r_{DS2}||r_{DS4} \cong 7.8$. As expected, this value is very low due to the characteristics of the transistor array used ($R_o \cong r_{DS2}||r_{DS4} \cong$ 4.2 kΩ). However, the gain remains sufficient for specific applications. The R_o value was derived from the OTA topology ($r_{DS2}||r_{DS4}$) using the datasheet information [14,15]. Experimental tests with the designed OTA confirmed the accuracy of these estimations with good precision.

The expected bandwidth can be calculated from overall transfer response:

$$K_{ampl}(s) = \frac{V_o(s)}{V_{in}(s)} \cong \frac{R_L}{\left(\frac{1}{g_{m1,2}} + R_S\right)}\cdot\frac{1}{(1 + sC_LR_L)} \quad (4)$$

as $f_{-3dB} \cong 1/(2\pi R_L C_L)$ that yields 1.3 MHz. Experimentally, the measured value was 1.1 MHz, which closely aligns with the theoretical prediction. Although the amplifier's gain is intentionally set below 1 (indicating attenuation), the results – particularly those in Fig. 4 – demonstrate good linearity in the response.

4. LC oscillator using degenerated OTA with very low output resistance

RC or active-C types of oscillators [9–10] that include multiple high-impedance nodes in their topology are unsuitable for the previously discussed degenerated OTA. This is due to the significant deviation between the theoretically expected and actual oscillation frequency and condition. Therefore, we selected an LC tank oscillator topology together with OTA. Although OTAs are not commonly used with real LC resonators, the presented topology does not suffer from the above-mentioned disadvantages (impact of R_o). The OTA amplifier discussed earlier has a very low and practically inapplicable output resistance ($R_o = r_{DS2}||r_{DS4} \cong$ 4.2 kΩ). Fortunately, this low value is not problematic when an appropriate design approach is adopted, including the careful selection of component values and application type. A typical example of such an oscillator is shown in Fig. 6. This LC oscillator consists of a single degenerated OTA (comprising 4 MOS transistors), two additional resistors, a diode limiter and an LC tank circuit. Despite their bulkiness, coils (inductors) are not an issue even for low-frequency designs because compact, through-hole technology (THT) inductors are readily available in standard component sizes. This type was selected for our case. The LC tank circuit consists of a parallel connection of a small coil and two capacitors (one fixed, one variable). The capacitor C_C (high value: 100 nF) serves as a decoupling capacitor, isolating the DC component V_{var} applied to adjust the oscillator. The capacitor C_i determines the initial oscillation frequency, while C_{var} (comprising two BB112 varactors [16] in parallel) provides oscillation frequency adjustment.

The varactor characteristics are plotted in Fig. 7. The capacitance of C_{var} can be varied approximately between 33 pF and 840 pF by adjusting the DC driving (reverse) voltage applied across the diode through an auxiliary high-value resistor. In an ideal case, the capacitance variation follows the function $C_{var} = C_{jo}/(1 + V_{var}/V_j)^M$, where $C_{jo} = 840$ pF is the

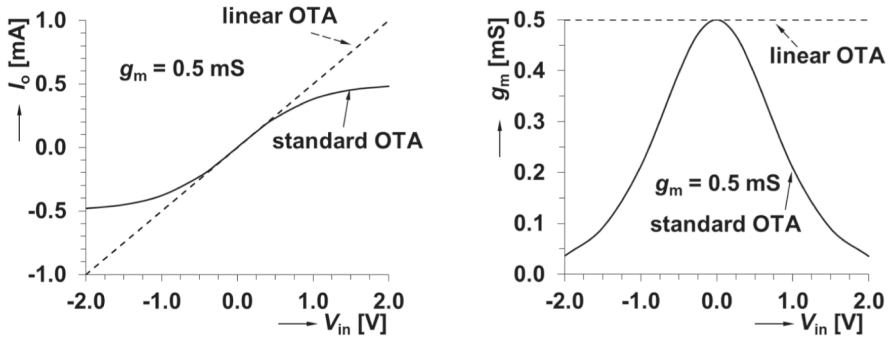


Fig. 3. Illustration of typical DC transfer response comparing standard (without linearization) and linear (ideal case) OTA: a) A-V response, b) transconductance vs input DC voltage.

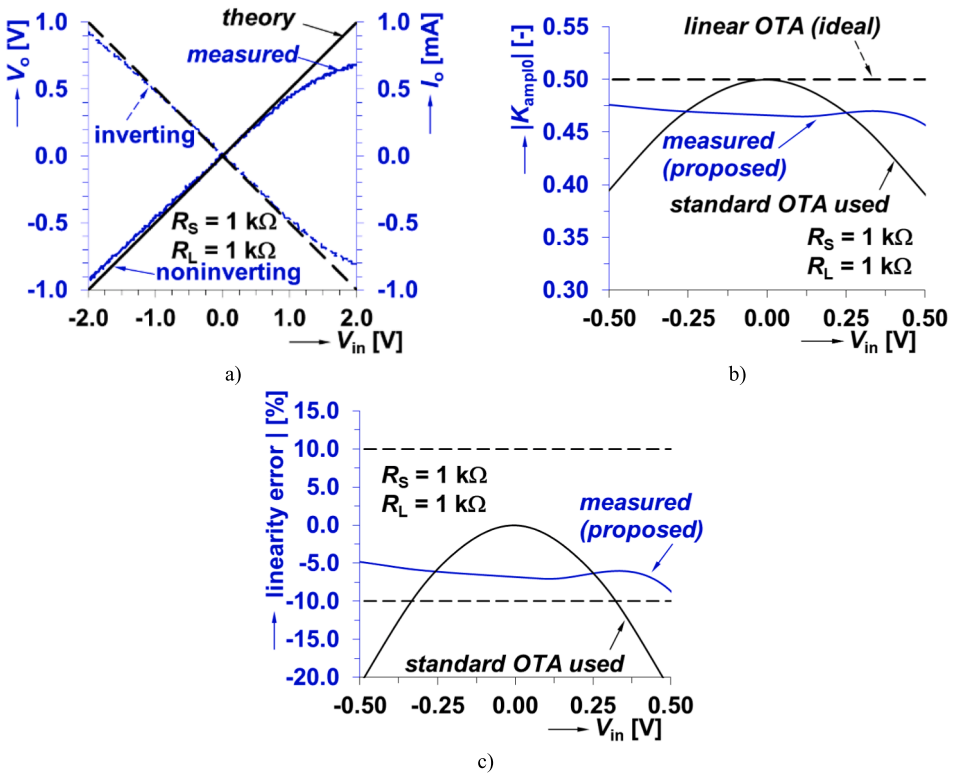


Fig. 4. The measured DC transfer response of the designed OTA and OTA-based amplifier/attenuator: a) input–output transfer responses, b) gain vs input voltage in detail, c) linearity error vs input voltage in detail.

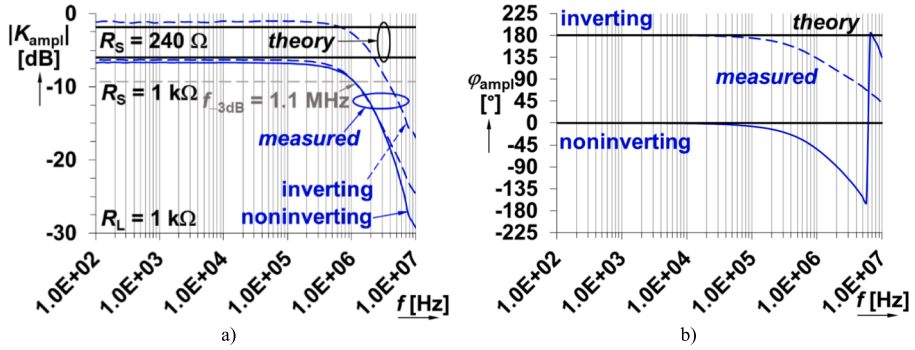


Fig. 5. The measured AC transfer response of the designed OTA amplifier/attenuator: a) magnitude responses, b) phase responses.

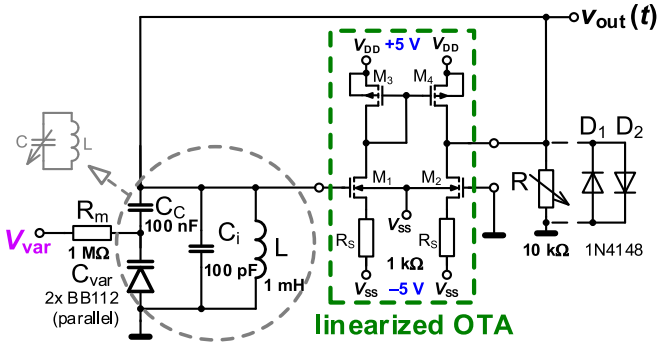


Fig. 6. The proposed LC voltage adjustable oscillator using degenerated OTA.

initial zero-bias PN junction capacity, V_{var} is the reverse bias/driving voltage, $V_j = 70$ V, is the PN junction potential and $M = 30$ is PN junction grading coefficient [18]. The maximum impedance value in Fig. 7**(b)** is defined by the auxiliary resistor R_m used in the testbed (see the subfigure of Fig. 7 **(a)**). Fig. 7 depicts the capacitance dependence up to its maximum allowed voltage $V_{var} = 8$ V. The resistor R is used to adjust the oscillation condition. Next, a diode limiter across R for a simple amplitude stabilization is used.

The key parameters of the oscillator circuit in Fig. 6 are defined by the characteristic equation:

$$s^2 + \frac{(R + R_0 - GM{\cdot}R{\cdot}R_0)}{R{\cdot}R_o{\cdot}(C_i + C_{var})}s + \frac{1}{L{\cdot}(C_i + C_{var})} = 0 \tag{5}$$

Since $C_C \gg C_{var}$, the effect of C_C in Fig. 6 can be omitted and the resulting formula for oscillation frequency has form:

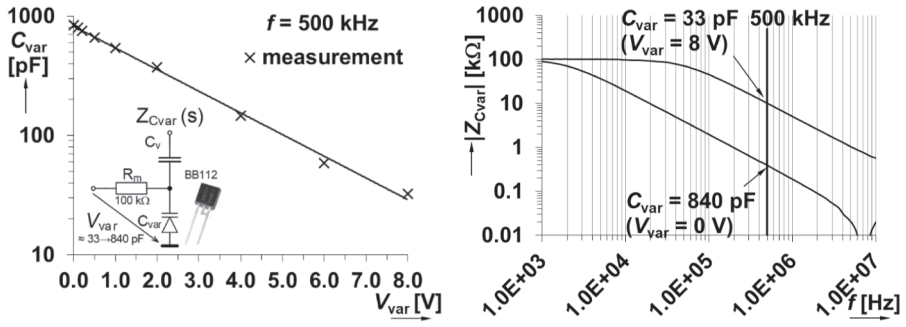


Fig. 7. The measured characteristics of the varactor BB112: a) the dependence of the capacity on the driving voltage, b) the impedance magnitude responses of the varactor for two limit values.

$$\omega_0 = \frac{1}{\sqrt{L\cdot(C_i + C_{var})}} \cong \frac{1}{\sqrt{L\cdot\left[C_i + \frac{2\cdot C_{jo}}{\left(1+\frac{V_{var}}{V_j}\right)^M}\right]}} = \frac{1}{\sqrt{L\cdot\left[C_i + \frac{2\cdot 840\cdot 10^{-12}}{\left(1+\frac{V_{var}}{70}\right)^{30}}\right]}} \tag{6}$$

The oscillation condition is given by $1/GM \leq R$. This very simple depends on the transconductance GM of the OTA and the grounded resistor R, which is advantageous for implementing an automatic amplitude stabilization system. However, since the degenerated (linearized) OTA operates with a fixed transconductance, continuous adjustment of GM is not possible. Additionally, higher GM values result in poorer linearity. For proper operation, the value of R should be significantly lower than the output resistance of OTA. To ensure precise f_0 tuning, an optocoupler (NSL-32SR3) [18] is used to replace R, as shown in Fig. 8. This solution stabilizes the output amplitude while maintaining an acceptable Total Harmonic Distortion (THD) level and stable output level.

The oscillator was designed to have an adjustable frequency range from 120 kHz to 240 kHz (adjustability ratio of 2). This range was achieved using $L = 1$ mH, $C_i = 100$ pF and two parallel varactors. The corresponding theoretical variation in capacitance ($C_i + C_{var}$) is from 310 pF to 1.78 nF. This capacitance variation is controlled by the tuning voltage V_{var}, which ranges from 0 to 5 V (with a supply voltage of ±5 V). Consequently, C_{var} varies approximately from 2·840 pF to 2·100 pF (two diodes in parallel). The intended operational band of the oscillator is not significantly influenced by stray capacitances created by the OTA terminals (especially the gate-source capacitances of the transistor elements in DIL packages). This capacitance reaches units of pF (approximately 3 pF, as reported in [14,15]), which when combined with several other elements, remains well below 10 % of the total LC tank capacity ($C_i + C_{var}$). The impact of these parasitic effects becomes more significant when the target operational band exceeds 500 kHz. Similar conclusions were confirmed by tests on a simple OTA-based amplifier, where the loading capacitance C_L was found/determined to affect the defined operational bandwidth (−3 dB), as discussed in Section 3.

The resistor R is selected in the kΩ range, making it comparable to or smaller than $R_o = 4.2$ kΩ. In the actual circuit, R is replaced by the optocoupler output, ensuring precise amplitude control when R_o and R are in parallel. The impedance of the optocoupler NSL-32SR3 [17] is

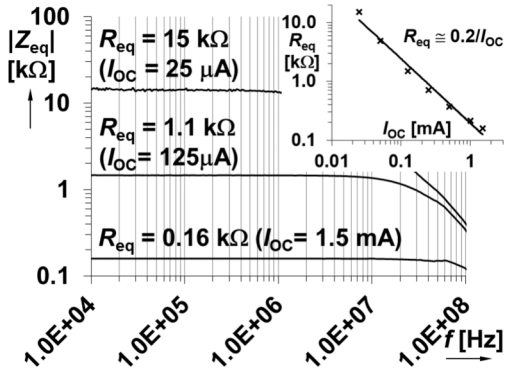


Fig. 9. The impedance plot of the optocoupler NSL-32SR3 (including the dependence of the real DC resistance on the bias control current).

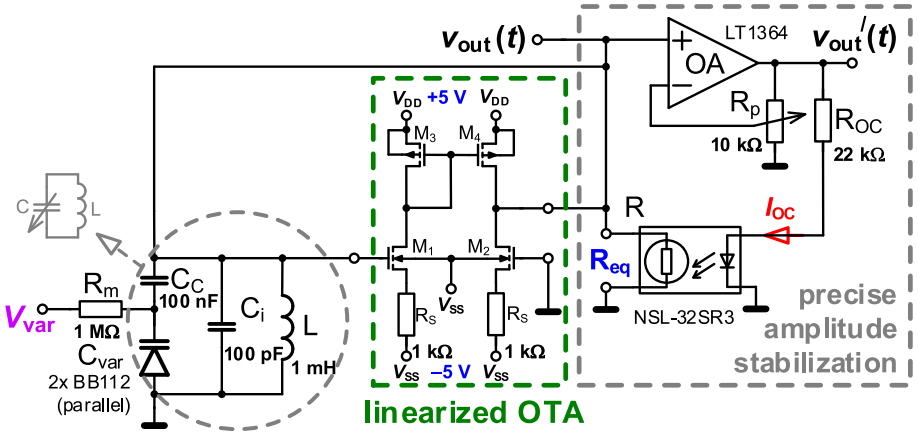


Fig. 8. The experimentally tested LC voltage adjustable oscillator using degenerated OTA and precise amplitude stabilization.

shown in Fig. 9. Its equivalent resistance (controlled by bias current I_{OC}) is given by $R_{eq} \cong 0.2/I_{OC}$. The amplitude stabilization derives I_{OC} from the output amplitude using an LT1364 operational amplifier [19].

Fig. 10 presents the experimentally obtained results, including oscillation frequency versus driving voltage, THD level versus oscillation frequency, and output amplitude versus oscillation frequency. The measured relative error between the expected and actual frequencies is within 6 % with an actual tuning range of 120 kHz to 273 kHz). The THD remains below 1.5 %, and the output peak-to-peak voltage is 200 ±20 mV across the tested frequency range. An example of the output waveform for $V_{var} = 0$ V (corresponding to the minimum oscillation frequency) and its spectral analysis (FFT) is shown in Fig. 11. All measurements were performed using a Keysight DSO-X 3024 T oscilloscope, which provided high-precision data recording and advanced analysis capabilities. The photo-documentation of tested breadboard and measuring equipment are shown in Fig. 12. A brief comparison of selected obtained experimental results and intended theoretical calculations of oscillation frequency from tuning range is given in Table 2.

5. Comparison of features of the oscillator application with similar solutions

Table 3 provides a brief comparison of recent electronically tunable oscillator designs and solutions that allow electronic adjustability [20]–[36]. Some of these solutions have not been fully verified [7,26,27]. Table 3 summarizes selected oscillator designs based not only on the OTA principles but also on more complex active devices that use OTA subparts in their construction. Most of these designs feature current outputs or auxiliary terminals, with the exception of the design presented in [36]. Many of the solutions in Table 3 are sensitive to the OTA's output performance, particularly the bias-controlled R_o. Specific values of this resistance can cause issues at the fulfilment of oscillation condition, as well as slight or significant inaccuracies in the generated oscillation frequency compared to theoretical calculations. The presence of such parasitic effects often leads to a dependence between the oscillation condition and the frequency, even in cases where theoretical analysis assumes these two parameters to be independent. Many solutions listed in Table 3 use the parameters of OTA (e.g., g_m) for electronic tunability of the application. However, typical standard OTA topologies, presented for example in [37] and [40], have a R_o value that depends on g_m (via bias control). Therefore, the tunability range, oscillation condition, and other performance characteristics can be affected by variations in R_o. As shown in Table 3, several designs produce very low signal levels, typically limited by the linearity constraints of the active devices (not using linearization/degeneration techniques) and by the low supply voltage [28,32–34,36].

Solution [36] offers the most similar characteristics and demonstrates potential adaptability when utilizing a low-performance active element. As previously noted, standard nonlinear active devices, such as standard CMOS OTA, work with only very small voltage levels when the waveform is not significantly distorted [20,26,28,30–34,36]. In contrast, our OTA solution benefits from source degeneration, which helps improve linearity and extend the usable voltage range. In terms of frequency adjustability, linearly adjustable oscillators—where two parameters vary simultaneously [9,32]—typically achieve higher adjustability ratios (f_{max}/f_{min}) than nonlinearly controlled oscillators (all other solutions in Table 3). In nonlinear designs, this ratio typically ranges between 1.3 and 5.5, with our design falling in the middle of this range. However, in our case, this ratio depends on the capacitor replacement method in the LC tank and varies based on the selected varactor type or similar tuning element.

A typical oscillator design using OTAs based on integrated CMOS elements was presented in [37]. The proposed topologies employ lossless and lossy integrators (three sections, i.e., 3–4 OTAs) in a single loop to generate various phase shifts between the output waveforms. However, electronic adjustment was achieved by varying the capacitor(s) values, enabling frequency tuning from several hundreds of Hz to a few MHz. Although the effect of bias current on the g_m (and thus on oscillation frequency) was tested, it was not shown in a separate figure.

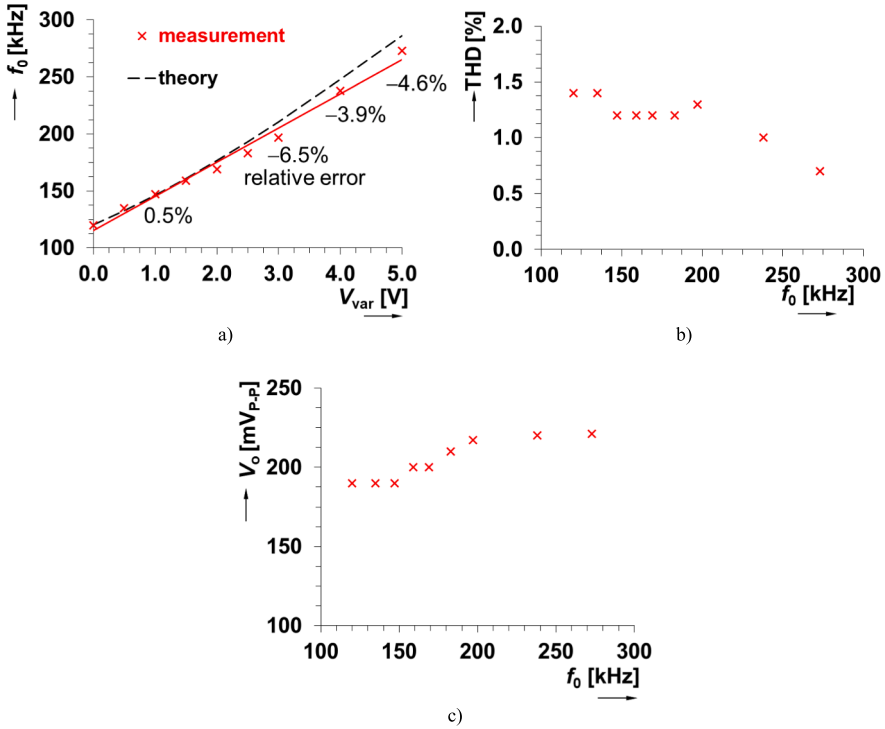
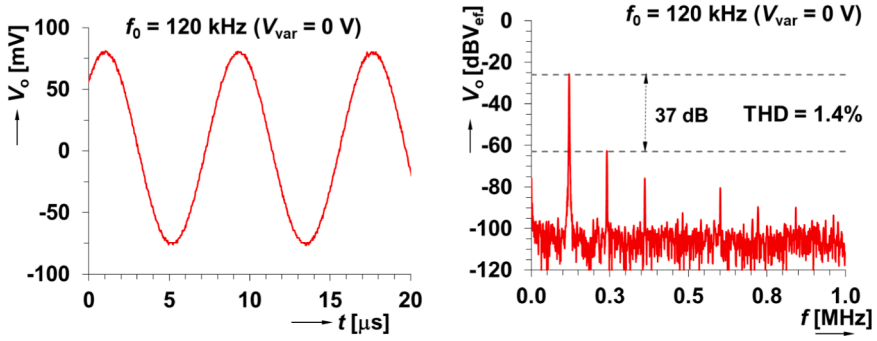
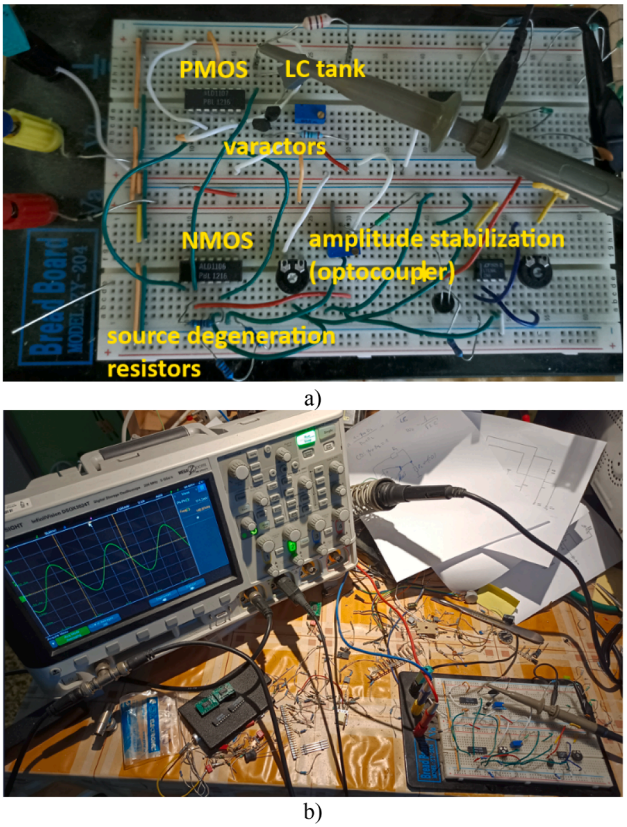


Fig. 10. The tunability characteristics of the designed LC oscillator: a) oscillation frequency vs driving voltage, b) THD vs oscillation frequency, c) output level vs oscillation frequency.



a) b)

Fig. 11. The analysis example of the generated waveform: a) time domain, b) FFT spectrum.



a)

b)

Fig. 12. Photo-documentation of the experiments: a) breadboard connection of the oscillator, b) the time domain measurement by oscilloscope.

Table 2
Comparison of selected calculated and measured data points from Fig. 10(a).

V_{var} [V]	f_0 [kHz] calculated	f_0 [kHz] measured	error [%]
0.0	119	120	+0.5
1.0	145	147	+1.0
2.0	176	169	−3.8
3.0	210	197	−6.0
4.0	247	238	−3.5
5.0	285	273	−4.2

Therefore, the tuning range obtained by electrically varying g_m was not mentioned. The results in [37] also indicate significant fluctuations in the generated output voltage. The most noteworthy aspect is the OTA topology itself. The OTAs used in [37] employ four CMOS elements with standard biasing of the differential pair, primarily for g_m control. In contrast, our approach uses emitter degeneration, whit no variation of the bias current expected in application. This ensures a fixed value of both g_m and R_o, while frequency tunability of application is solved through a different method.

The topologies reported in [36,38,39] also offer advantages in minimizing parasitic effects in active devices (an impacts of R_o), as they do not use active elements with current output terminals. However, the concept of electronic tunability is not directly employed in [38,39], and topologies require more than a single active device.

6. Conclusion

This paper presented a design approach based on commercially available active devices having several performance limitations created by the manufacturer, particularly low output resistance in this case. The results indicate that specific implementations of such devices can be advantageous, their disadvantages can be mitigated by careful circuit design and topology selection. When the design limitations are known, it is possible to select appropriate circuit topologies and complementary component values to effectively compensate for these limitations.

A linearized OTA, utilizing only four MOS elements with low drain-source resistance, was chosen as a typical example. Its implementation into a specific LC oscillator topology successfully minimizes the impact of its disadvantages. The OTA-based voltage amplifier works with linearity error below 8 % within an input range of ±0.5 V, producing an output current of ±250 µA and achieving a bandwidth > 1 MHz. While the high-impedance current output terminal has a resistance of 4.2 kΩ (which limits gain), this does not limit its usability in a simple, electronically adjustable LC oscillator with a specialized topology.

The oscillation frequency is tunable between 120 kHz and 273 kHz via a DC driving voltage (from 0 V to 5 V), while maintaining acceptable distortion levels below 1.5 % and a stable output amplitude. These findings demonstrate that devices with problematic performance characteristics can still be effectively used in specific applications, addressing the research question posed in this work. Additionally, our work validates the feasibility of LC oscillator, even in frequency bands typically dominated by RC or active-RC solutions, without suffering from the drawbacks of bulky or heavy inductors, thanks to the use of modern components.

Beyond the presented results, there are alternative approaches that involve entirely different active devices (e.g., [38,39]). Operational amplifiers, which are among the most widely used active elements in custom oscillator designs, are gaining popularity. Unfortunately, the variable voltage gain, which enables oscillation frequency tuning, must be implemented by resistor feedback [36] which complicates voltage tuning.

The importance of bias/gain control of the OTA stage on further

Table 3
Comparison of oscillators showing feature of electronically adjustable frequency and mutually independent oscillation condition without consideration of auxiliary circuits (amplitude stabilization, bias transformers, etc.).

Reference	Number of active elements	The simplest active device (s) (not covering several active devices)	Number of passive elements (except active device)	Electronic adjustment of oscillation frequency (type)	Tested tunability range ratio (f_{max}/f_{min})	Stable output level (average of available amplitude in form of voltage or current)	Multiphase (multi-output) solution	Maximal reported THD	Power consumption	Experimental laboratory test of electronic tunability
[7]	2	No	5	linear	N/A	200 mV	Yes	N/A	5 mW	No
[9] Fig. 5	3–4	Yes	2–3	linear	55	100 mV	Yes	0.3	N/A	Yes
[20]	1	No	3	nonlinear	3.5	70 mV	Yes	2.9	1.3 mW	No
[21]	2	No	4	linear	4.5	4 V	Yes	N/A	N/A	Yes
[22]	2	Yes	3	nonlinear	1.4	100 mV	Yes	1.5	N/A	Yes
[23]	3	Yes	5	linear	2.8	2 V	Yes	1.7	N/A	Yes
[24]	1	No	3	nonlinear	5.5	300 mV	Yes	0.9	1.1 mW	No
[25]	1	No	4–6	nonlinear	1.2	50 μA	Yes	>10	N/A	Yes
[26]	5	Yes	2	linear	N/A	70 mV	Yes	N/A	N/A	No
[27]	2	No	4	linear	N/A	150 mV	Yes	3.0	2 mW	No
[28]	3–4	Yes	2	nonlinear	3.2	20 mV	Yes	3.9	960 mW	Yes
[29]	3	No	3	nonlinear	4.2	150 mV	Yes	1.1	1 mW	Yes
[30]	4	Yes	3	linear	2.0	70 mV	Yes	1.3	N/A	Yes
[31]	3	Yes	3	nonlinear	3.3	70 mV	Yes	0.5	N/A	No
[32]	5	Yes	2	linear	30	30 mV	Yes	3.8	N/A	Yes
[33]	4	Yes	2	nonlinear	3.2	40 mV	Yes	3.8	1200 mW	Yes
[34]	4	Yes	2	nonlinear	4.3	15 mV	Yes	0.9	N/A	Yes
[35]	1	No	3	nonlinear	2.6	100 μA	No	N/A	N/A	No
[36]*	1	Yes	4	nonlinear	1.3	35 mV	Yes	N/A	N/A	No
Proposed Fig. 6	1	Yes	6	nonlinear	2.3	100 mV	No	1.4	70 mW	Yes

*This work presents several solutions using voltage mode device (voltage amplifiers with almost zero output resistance), frequency adjustment is external (not aimed at parameters of active element).
N/A – not available, not tested, not verified, not shown.

performance (as output impedance) has been highlighted in [40] as it brings signification issue especially with decreasing size of transistors in modern CMOS fabrication technologies.

CRediT authorship contribution statement

Roman Sotner: Writing – review & editing, Writing – original draft, Visualization, Validation, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Ladislav Polak:** Writing – review & editing, Writing – original draft, Validation, Formal analysis, Data curation, Conceptualization. **Lukas Langhammer:** Writing – review & editing, Writing – original draft, Validation, Supervision, Formal analysis. **Darius Andriukaitis:** Writing – review & editing, Writing – original draft, Validation.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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