Analysis of Smart Power Sockets Implementation

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Abstract—**In this paper an analysis of implementation alternatives of smart electrical power sockets is presented. Smart socket (SSoc) functionality include power measurement, wireless connectivity, and load control. Power measurement uncertainty is defined by SSoc design and calibration. We investigate influence of voltage and current waveforms quantization errors and influence of Hall current sensor noise upon the active power measurement uncertainty. Voltage and current measurement module is calibrated by estimating corresponding gain factors using reference power analyser. Then calibration errors influence upon power measurement errors is studied. SSoc internal power dissipation is analysed by means of alternative power supply modules prototyping.**

Index Terms—**Smart socket, power measurement, uncertainty, calibration, Hall sensor.**

I. INTRODUCTION

Emergence of specialized, low power, cheap, and small size electronic components enabling electrical power measurement and wireless connectivity together with the rise of IoT (Internet-of-Things) paradigm made so called smart electric sockets an attractive research and development topic and affordable node for home automation and energy management solutions [1]–[5]. Basically, a smart socket (later SSoc) or a smart plug (outlet, strip) is aimed to measure electrical power consumption, to give access to power readings and to allow control (switch on/off) of loads in a remote (wireless) manner. Services supported by SSoc systems include energy management, load control, consumption profile monitoring, home automation, appliances faults diagnostics, *etc*. Wireless channel is used either for connection to IoT/home automation gateway or for local human machine interface via smart phone or tablet PC. It is expected that SSoc will play a significant role as consumer end-device in Smart grids deployment. Various SSoc implementations, architectures and applications are described in [1]–[9].

Most of the described SSoc implementations focus on wireless connectivity implementation but pay much less

attention to achievable power measurement uncertainty [3], [4], [6], [7], [9]. Power measurement accuracy of around one 1 % after calibration is reported in [3], [4], [7], but accuracy characterization over measured power range is never considered. However, power measurement accuracy reduction in lower range of power consumption could be of crucial importance leading to ineffective energy saving policies (based on inaccurate measurements), since many appliances spend most of the time in standby mode. Though power measurement errors of electronic electricity watt-meters are extensively studied, but restrictions on SSoc size and cost result in innovative solutions with less investigated power measurement uncertainty budgets. Therefore, estimating power measurement uncertainty and identifying main uncertainty sources is important for guiding new SSoc designs. Our research contribution provides analytical uncertainty analysis for the proposed SSoc implementation. Another issue not addressed by most of the authors is the energy efficiency of a SSoc itself. To make SSoc economically reasonable it is preferably to keep their power dissipation at the level below of standby power of controlled appliances. Our second research goal then is to verify which power supply module implementations allow to meet this requirement.

In Section II we give an overview of the state-of-the-art in SSoc implementation options, summarize requirements, provide analysis of power measurement uncertainty, and power supply module alternatives comparison.

II. IMPLEMENTATION ANALYSIS AND TESTING

A. Requirements, Architecture and Functionality Mapping

A typical SSoc is composed of measurement, connectivity, load control and power supply subsystems. The key requirements for a SSoc include small dimensions (could be mounted inside of wall or connected between wall socket and load's power cord), minimal power losses, low measurement uncertainty including standby power range, pricing constraints and wireless connectivity inside residential buildings.

SSoc implementation is usually based on a low power embedded microcontrollers (MC) [2], [4], [5], [7]. Indeed, the functionality including all layers of wireless stack, device control and digital processing of measurement results is difficult to achieve without a programmable or application specific device.
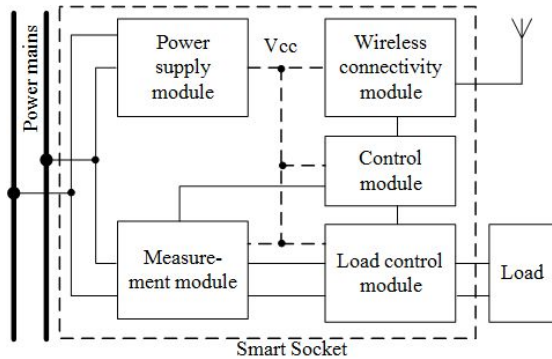

Fig. 1. Block diagram of smart socket architecture.

The most often scenarios of SSoc architectural blocks mapping to present day integrated semiconductor circuits (IC) are listed in Table I. Application specific integrated circuits (ASIC) or analog front-ends (AFE) have inputs for sensed current and voltage. Rogowski coil, current transformer [3], [9], Hall effect current sensor [1] or shunt resistor [10] is traditionally used for current sensing, while step-down voltage transformer [3] or resistive divider [9], [10] can serve as voltage sensing circuit. Examples of power metering ASIC/AFE are Analog Devices ADE7816, STMicroelectronics STPMxx, Cirrus Logic CS54xx [9], Linear technology LTC2946, Microchip MCP3909, Atmel M90Exx, *etc*. Examples of SoCs containing embedded MC with power estimation modules or DSP are Teridian/Maxim 71M654xx, Texas Instruments MSP430FE42xx, NXP Semiconductors EM783, *etc*.

TABLE I. SCENARIOS OF FUNCTION MAPPING TO IC.

Scenario	Function (block in architecture)		
	Measurement/ calculation	Wireless connectivity	Control
S1	ASIC/AFE	NP	NP
S2	ASIC/AFE	Transceiver	Embedded MC
S3	Embedded MC SW	NP	NP
S4	Embedded MC SW	Transceiver	Embedded MC
S5	MC-PEDSP	Transceiver	MC-PEDSP

Note: 1) ASIC/AFE -Power metering ASIC or analog front-end (AFE),
2) NP - Network processor (Embedded MC with integrated transceiver),
3) MC-PEDSP - MC with integrated Power Estimation DSP.

To our knowledge, a SoC integrating embedded MC, power metering ASIC/AFE together with wireless transceiver is absent in the market at the moment of the paper writing. Therefore, for scenarios S3 and S4 electrical power calculations from voltage and current waveforms must be implemented in MC software.

A SSoc is most often equipped with Zigbee [3]–[5], [7], [10], WiFi [2], or Bluetooth [9] wireless connectivity. Wireless connectivity can be implemented using either IP oriented protocol stacks like 6LoWPAN, WiFi, or using non-IP standard protocol stacks such as Zigbee, XBee, WirelessHART, wM-Bus, Bluetooth or proprietary stacks like SimplicityTI [11]. IP oriented protocols require to run a

more complex communication stack on the embedded MC, and therefore are less preferable.

B. Applied Power Measurement Technique

For the further analysis we investigate implementation scenarios S3 and S4, utilizing Hall sensor for current sensing and step-down transformer for voltage sensing (Fig. 2). Advantages of Hall sensor are small dimensions and galvanic isolation between high and low voltage domains. High internal noise level of Hall sensor is the obvious drawback, but its influence upon current and power measurement uncertainty was little investigated before. A possible Hall sensor available in the market from Avago is ACS712ELC-20A.
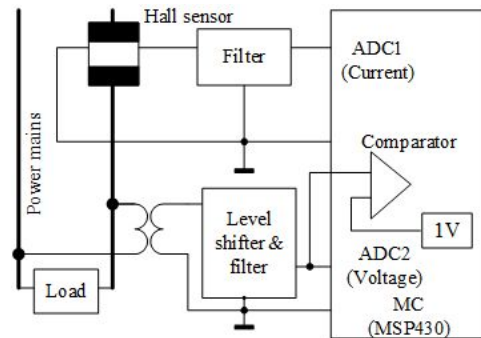

Fig. 2. Current and power sensing in SSoc prototype.

Instantaneous load current is described by the expression

$$I = g_I \times (V_{IADC} - V_{Ioffset}), \qquad (1)$$

where V_{IADC} is measured voltage at the current channel ADC input, $V_{Ioffset}$ is offset voltage estimated by averaging sampled voltage waveform over the network voltage waveform period using MC software. Gain coefficient g_I is estimated by calibrating current measurement circuit using reference Power Analyzer (PA) Yokogawa WT310 as shown in Fig. 3. Calibration errors are shown in Fig. 4.
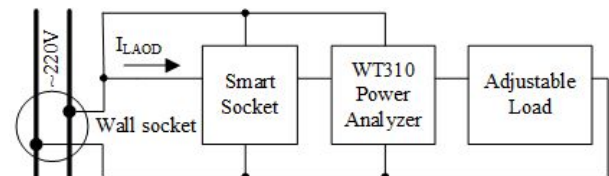

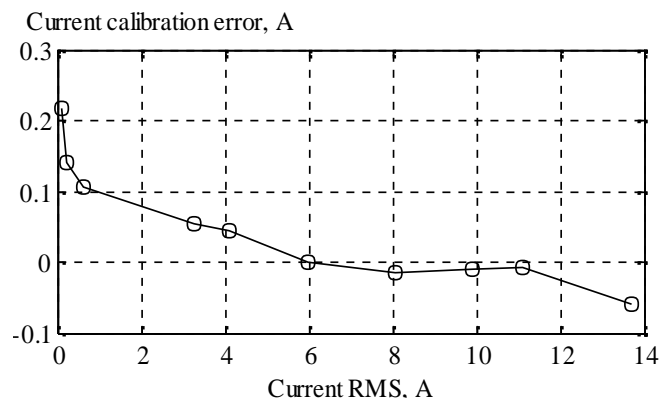Fig. 3. Voltage and current calibration and power measurement verification setup.

Fig. 4. Current calibration errors vs. current RMS value.

Instantaneous measured network voltage is described by the expression

$$V = g_V \times (V_{VADC} - V_{Voffset}), \qquad (2)$$

where V_{VADC} is voltage at the ADC input, $V_{Voffset}$ is voltage level defined by level shifter, and g_V is transformation coefficient encountering for transformer ration, level shifter and filter circuit attenuation.

Value of $V_{Voffset}$ is determined by averaging sampled voltage waveform over the network waveform period. Value of g_V is obtained by calibrating voltage measurement circuit. The reference point is selected at current RMS value equal to 6 A. Although the most often power meter's active power measurement is calibrated, in this research we choose to calibrate voltage and current separately. This approach allows us to perform analysis of current and voltage measurement uncertainties influence upon active power measurement uncertainty.

Voltage and current sampling and quantization is done using single ADC of embedded MC CC430F6137. Therefore, sampling moments of current and voltage are shifted by one sampling period. To minimize power uncertainty due to this shift, the average active power is calculated according to the expression

$$P_A = \frac{1}{N} \sum_{i=0}^{N} \frac{I(t_{i-1}) + I(t_{i+1})}{2} \times V(t_i), \qquad (3)$$

where $N = round(p \times T_{Net} / T_S)$, $T_{Net} = 20\,ms$ is AC network voltage period, $T_S = 100 \sim s$ is sampling period, and p is the number of power network fundamental periods used for power estimation. AC network voltage period start and end moments are detected using MC's internal comparator with the internal programmable reference level set to 1 V (Fig. 2).

C. Power Measurement Uncertainty Analysis

Uncertainty of active power $u(P_A)$ is described by applying uncertainty propagation law to (3)

$$u(P_A) = \sqrt{\sum_{i=1}^{N} \left(\left(\frac{\partial P_A(t_i)}{\partial I(t_i)} \right)^2 u_I^2 + \left(\frac{\partial P_A(t_i)}{\partial V(t_i)} \right) u_V^2 \right)}, \qquad (4)$$

where u_I is current measurement uncertainty, and u_V is voltage measurement uncertainty.

Assuming $(I(t_{i-1}) + I(t_{i+1}))/2 \approx I(t_i)$ in (3), the (4) can be rewritten

$$u(P_A) = \sqrt{\frac{1}{N^2} \sum_{i=1}^{N} \left(V^2(t_i) u_I^2 + I^2(t_i) u_V^2 \right)}. \qquad (5)$$

We do not deny other major sources of power measurement uncertainty, namely ADC reference voltage stability, antialiasing or noise filter, temperature, *etc.*, but in the current research we focus on comparing contributions caused by limited number of current and voltage quantization bits and Hall sensor noise. Quantization caused current and voltage measurement uncertainties are estimated accordingly:

$$u_{Iq} = \Delta_I / \sqrt{3}, \qquad (6)$$

$$u_{Vq} = \Delta_V / \sqrt{3}, \qquad (7)$$

where one bit corresponding current and voltage steps are:

$$\Delta_I = g_I \frac{V_{REF}}{2^{12} - 1}, \qquad (8)$$

$$\Delta_V = g_V \frac{V_{REF}}{2^{12} - 1}, \qquad (9)$$

where $V_{REF} = 2.5\,V$ is reference voltage of ADC.

Though the specified internal Hall sensor noise peak-to-peak value is $21\,mV$, but noise RMS value measured at the output of filter (Fig. 2) is $V_{Hn} = 0.9\,mV$. The first order filter's cut-off frequency defined at the -3 dB point is 4 kHz. The corresponding uncertainty is then $u_{In} = V_{Hn} / \sqrt{3}$.

Considering only quantization errors and Hall sensor noise, current and voltage uncertainties are:

$$u_I = \sqrt{u_{Iq}^2 + u_{In}^2}, \qquad (10)$$

$$u_V = u_{Vq}. \qquad (11)$$

Since voltage and current root mean square (RMS) values are defined by:

$$V_{RMS}^2 = \frac{1}{N} \sum_{i=1}^{N} V^2(t_i), \qquad (12)$$

$$I_{RMS}^2 = \frac{1}{N} \sum_{i=1}^{N} I^2(t_i), \qquad (13)$$

then (5) can be rewritten

$$u(P_A) = \sqrt{\frac{1}{N} \left(V_{RMS}^2 u_I^2 + I_{RMS}^2 u_V^2 \right)}. \qquad (14)$$

Nominal network voltage RMS value is $V_{RMS} = 220\,V$, while nominal current RMS value depends upon consumed power P_{Anom}.

As can be seen from Fig. 5, active power measurement uncertainty cannot be significantly reduced by increasing ADC resolution above 12 bits. This indicates that above 12 bits ADC resolution, the uncertainty is dominated by the Hall sensor noise. Options for the uncertainty reduction can include increase of voltage and current sampling frequency and increasing number of network fundamental periods used for averaging according to (3). On the other hand increasing of sampling frequency is not favourable from MC power consumption perspective.
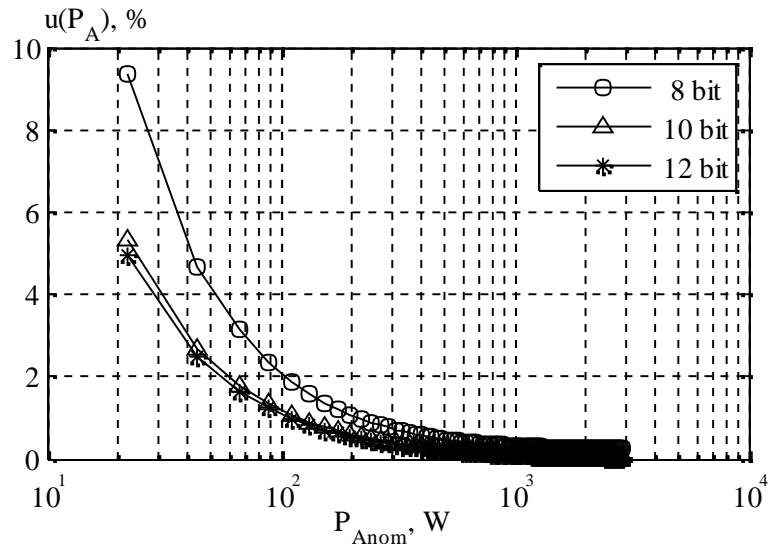
Fig. 5. Power measurement uncertainty (number of averaged periods p = 1).

A. Power Measurement Verification

Verification of power measurement implementation is carried out using the setup shown in Fig. 3. SSoc is calibrated at 6 A current and 220 V voltage RMS levels using the same reference instrument. Then calibration coefficients are included in active power calculation according to (1)–(3). The observed differences between reference instrument readings and measurement results produced by the software of SSoc prototype are shown in Fig. 6. In the lower range of measured power the relative error increases heavily, indicating domination of current measurement module calibration errors (see also Fig. 4). Indeed, error in Fig. 6 does not follow hyperbolic law, which is characteristic for constant errors like quantization and Hall sensor noise. This suggests that more complex calibration procedure including shift coefficient (not only gain) estimation would be beneficial seeking to reduce overall power measurement uncertainty.
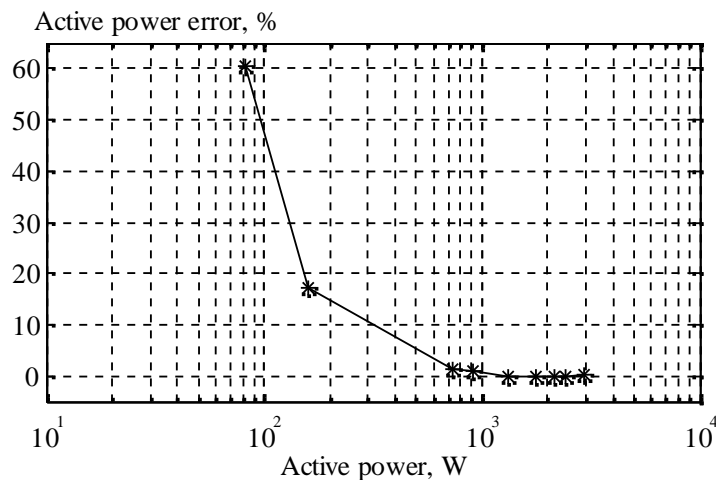

Fig. 6. Active power measurement errors.

A. Power Supply Subsystem Prototyping

Requirements for a SSoc power supply module include minimization of dimensions, minimization of power losses and output voltage noise in order to reduce its impact upon ADC reference voltage source. Power dissipation is of the key importance because the socket itself is full day operated and should add a negligible energy overhead in order to be economically justifiable. The total SSoc power dissipation at least should not exceed the requirements for standby power of consumer equipment, which is less than 0.5 W according to European Commission eco design for standby and off mode regulation (page 6) [12].

We experimentally investigate four typical power supply module implementation scenarios: three fly-back topology AC-DC converters (based on switching regulators NCP1072 from ON-Semiconductor, Viper17H from STMicroelectronics, and modular AC-DC converter VTX-214-001-105 from Vigortronix, and one AC-AC transformer (HAHN BV-201-0142) based implementation (see TABLE II). All of them proved similar performance, indicating around $\eta = 30$ % efficiency at the nominal (including Hall sensor consumption, SoC with transceiver alternating between transmit and receive modes) SSoc power dissipation $P_{SSoc} = 110$ mW.

TABLE II. POWER SUPPLY MODULE ALTERNATIVES.

Parameter	SMPS NCP1072	SMPS Viper17H	SMPS VTX-214-001-105	AC-AC transformer BV-201-0142
P_{in}, mW	370	340	360	1570
P_{SSoc}, mW	110	110	110	170
Ƞ, %	30	32	30	11
Size, cm^3	21	30	10.4	8.5
Ripple V, mV	12	30	104	18
BoM, €	7.2	8.1	6.0	4.6

SMPS based on VTX-214-001-105 converter is preferable for SSoc design in terms of cost-size-power dissipation ratio. Higher level of ripple voltage is less important because ADC reference voltage is generated by internal MC reference source, but not directly from power supply. However, more detail investigation concerning ripple level impact on measurement uncertainty should be done in future.

III. CONCLUSIONS

1. Wireless microcontroller with integrated power consumption measurement front-end could facilitate designing smart power sockets by means of dimensions and power measurement uncertainty reduction. However, this type of SoC is not available on the market today.

2. Current Hall sensor internal noise caused errors dominate power measurement uncertainty budget compared over 12 bit voltage and current quantization errors, especially in low power range.

3. Only current and voltage gain (without offset) calibration causes a significant increase of power measurement errors below several hundreds of watts.

4. Switched mode power supply with power dissipation less then EU eco design directives guided standby power is achievable using state-of-the-art AC-DC converters.

REFERENCES

[1] F. Nakazawa, H. Soneda, O. Tsuboi, *et.al,* "Smart power strip network and visualization server to motivate energy conservation in office", *9th IEEE Int. Conf. Industrial Informatics (INDIN),* pp. 352–357, 2011. [Online]. Available: http://dx.doi.org/10.1109/indin.2011.6034901

[2] G. Galioto, N. Galioto, C. Giaconia, *et.al*, "Smart plugs: A low cost solution for programmable control of domestic loads", *AEIT Annual Conf.*, 2014, pp. 1–6. [Online]. Available: http://dx.doi.org/10.1109/aeit.2014.7002015

[3] S. Hussain, M. J. Ikram, N. Arshad, "A low cost implementation of home area networks for home energy management systems", *IEEE Fourth Int. Conf. on Big Data and Cloud Computing*, pp. 688–695, 2014. [Online]. Available: http://dx.doi.org/10.1109/bdcloud.2014.58

[4] E. Spano, L. Niccolini, S. D. Pascoli, G. Iannaccone, "Last-meter smart grid embedded in an Internet-of-Things platform", *IEEE Trans. Smart Grid,* vol. 6, no. 1, pp. 468–476, 2015. [Online]. Available: http://dx.doi.org/10.1109/TSG.2014.2342796

[5] Mon-Chau Shie, Po-Chen Lin, Tsung-Mao Su, Poki Chen, A. Hutahaean, "Intelligent energy monitoring system based on ZigBee-equiped smart sockets", in *Proc. 2014 Int. Conf. Intelligent Green Building and Smart Grid (IGBSG),* Taipei, 2014, pp. 1–5.

[6] A. S. Kulkarni, K. C. Welch, C. K. Harnett, "A review of electricity monitoring and feedback systems", in *Proc. IEEE Southeastcon*, Nashville, TN, 2011, pp. 321–326.

[7] Jiho Kim, Wan-Hee Cho, Yongjin Jeong, Ohyoung Song, "Intelligent energy management system for smart offices", in *Proc. IEEE Int. Conf. Consumer Electronics (ICCE),* Las Vegas, NV, 2012, pp. 668–669.

[8] Smart Outlet Handbook. [Online]. Available: http://postscapes.com/smart-outlets

[9] R. Makwana, J. Baviskar, N. Panchal, D. Karia, "Wireless based load control and power monitoring system", *Int. Conf. Energy Efficient Technologies for Sustainability (ICEETS)*, 2013, pp. 1207–1211. [Online]. Available: http://dx.doi.org/10.1109/iceets.2013.6533559

[10] Lih-Jen Kau, Bi-Ling Dai, Chih-Shen Chen, Sung-Hung Chen, "A cloud network-based power management technology for smart home systems", in *Proc. IEEE Int. Conf. on Systems, Man, and Cybernetics (SMC),* Seoul, 2012, pp. 2527–2532. [Online]. Available: http://dx.doi.org/10.1109/icsmc.2012.6378125

[11] G. Reiter, "Wireless connectivity for the Internet of Things", White Paper by Texas instruments, 2014.

[12] Commission Regulation (EC) No 1275/2008. [Online]. Available: http://eur-lex.europa.eu/legal-content/EN/ALL/?uri=CELEX:32008R1275