Reconnection–less Reconfigurable Fractional–Order Current–Mode Integrator Design With Simple Control

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ABSTRACT A design of a fractional-order (FO) integrator is introduced for the operation of the resulting solution in the current mode (CM). The solution of the integrator is based on the utilization of RC structures, but in comparison to other RC structure based FO designs, the proposed integrator offers the electronic control of the order. Moreover, the control of the proposed integrator does not require multiple specific and accurate values of the control voltages/currents in comparison to the topologies based on the approximation of the FO Laplacian operator. The electronic control of a gain level (gain adjustment) of the proposed integrator is available. The paper offers the results of Cadence IC6 (spectre) simulations and more importantly experimental measurements to support the presented design. The proposed integrator can be used to build various FO circuits as demonstrated by the utilization of the integrator into a structure of a frequency filter in order to provide FO characteristics.

INDEX TERMS Current–mode, electronic control, fractional–order, fractional–order emulator, frequency filter, integrator, reconnection–less reconfiguration.

I. INTRODUCTION

The research of fractional–order (FO) systems and circuits became an important and widespread area of interest in the last decade. This is due to the fact that FO systems can offer the ability to follow the required parameters more accurately and thus to extend possibilities of different applications in comparison to the integer-order systems. Fractional–order systems have found their application in diverse industry branches such as medicine [1], [2], modeling and measurement of various signals [3]–[5], agriculture [6], car industry [7], etc. In case of the electrical engineering, the utilization of FO calculus covers circuits filtering the spectrum [8]–[17], FO oscillators [18]–[23] and other circuits with fractional–order characteristics [24]–[29], which then can be implemented and find their purpose in applications of above–mentioned industry areas.

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There are different ways how to approach the design of FO circuits and systems. The most common way uses so–called Fractional–Order Elements (FOEs). The FOE represents a non–integer element with its behavior between either a standard resistor and capacitor with the resulting impedance given as $Z_C = 1/s^\alpha C_\alpha$ [30], or a standard resistor and inductor with the resulting impedance of $Z_L = s^\alpha L_\alpha$ [31], where s^α is fractional–order Laplacian operator, C_α is a pseudo–capacitance in Farad/sec$^{1-\alpha}$ and L_α is a pseudo–inductance in sec$^{1-\alpha}$/Farad. The phase shift of such element is given by $\pm 90 \times \alpha$ degrees, where α is a real number in range $0 < \alpha < 1$.

The FOEs are available in various forms. Some of these realizations are based on the physical implementation of these elements [32]–[34]. This approach has a disadvantage of commercial unavailability of these realizations and the absence of the electronic control of the resulting order. The next approach involves the substitution of the FOE by RC ladder networks [11], [13]–[17]. RC structures offer the

possibility of simple design due to the commercial availability of building elements (only require common capacitors and resistors). The disadvantage is that the electronic control of the order is not available (the values of resistors and capacitors of the RC structure vary based on the desired FO and thus the resistors and capacitors of the RC structure need to be changed, or whole RC structure has to be redesigned and replaced). The last common technique is using emulators exhibiting specific behavior of the FOE [35]–[39]. The structure of these emulators is usually more complex and requires active elements in comparison to the previous approaches nonetheless, they often offer the electronic control of some parameter (fractional order, frequency band where the FO approximation is valid, gain adjustment, etc.).

A slightly different approach to the design of FO circuits is a proposal of FO integrators and differentiators [40]–[49]. In comparison to the FOE emulators, which provide the function of a FO impedance, the FO integrators and differentiators serve as FO building blocks as they offer a FO transfer function rather than work as a FO impedance. These FO building blocks can be used to design diverse FO circuits by a simple replacement of whole building block (integer–order integrator or differentiator) of an integer–order circuit. There are a few variations of FO integrators/differentiators. Those introduced in [40]–[42] are based on the utilization of RC structures and thus, they do not allow the electronic control of the order (they still might offer the electronic control of other parameters such as the adjustment of the gain level of the output response). The change of the order is achieved by the replacement of the RC structure specifically calculated to provide results of the desired order. The solution in [43] does not offer the electronic control of the order neither the electronic control of any other parameter unless the active elements used in the design have a feature of the electronic adjustment of some parameter (not the case of the discussed design). The change of the order can be achieved by the replacement of passive parts of the structure. The FO building blocks in [44]–[49] do offer the electronic control of the resulting fractional order and possibly the electronic control of other parameters as well. Nevertheless, the control of these structures can be rather complex and problematic (further discussed in chapter V).

This text presents a design of a fractional-order integrator. The design of a FO integrator working in the current mode (CM) is offered. The solution provides a simple electronic control of the order and gain adjustment in comparison to other previously introduced integrator/differentiator designs. The design is based on a chip developed in CMOS I3T25 0.35 μm ON Semiconductor process offering multiple operational cells within. The introduced proposal is supported by Cadence IC6 (spectre) platform simulations alongside with experimental measurements of the implemented structure. A possible utilization of the proposed FO integrator in an application is shown for a $1 + \alpha$ (see equation (4)) frequency filter design.

The paper has the following organization: section I provides a background for the discussed matter. Section II introduces the proposed CM FO integrator which is then followed by the part (section III) showing the simulation and experimental results of this integrator. A possible utilization of the proposed CM FO integrator in a FO filter is shown in section VI. Discussion and comparison of the introduced design, in comparison to other previously presented solutions, is given in section V. The paper is concluded by section VI – the conclusion.

II. CURRENT–MODE FRACTIONAL–ORDER INTEGRATOR PROPOSAL

The design of the proposed integrator is based on the utilization of a chip introduced in [50]. The chip is implemented in CMOS 0.35 μm I3T25 ON Semiconductor technology. It contains several analogue cells, namely a second–generation current–controlled current conveyor (CCCII) with four outputs, current amplifier (CA), voltage multiplication units (MLTs) with a current output (one in CMOS and one with a bipolar core) and a voltage differencing differential buffer (VDDB). The transistor–level topologies of individual active elements are available in [50]. The presence of multiple cells in the chips allows a modular interconnection of these cells in order to construct diverse circuits or advanced active elements with multiple electronically controllable features.
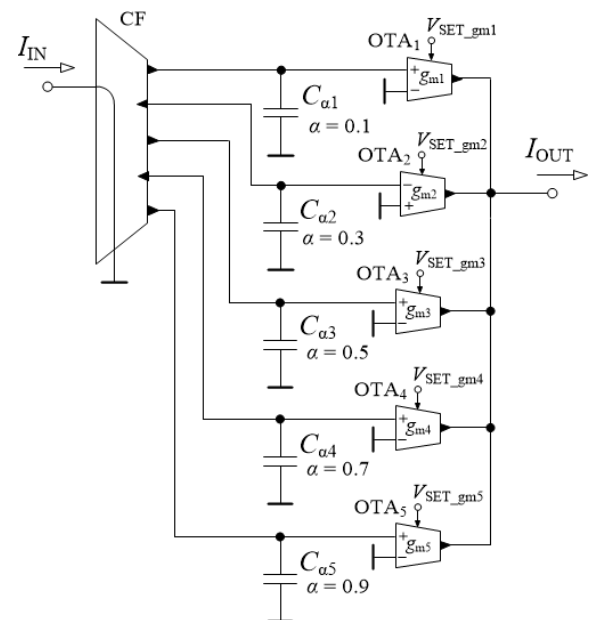

FIGURE 1. Proposed current–mode fractional–order integrator.

The proposed CM FO integrator is depicted in Fig. 1. The structure involves one current follower (CF) and a number of operational transconductance amplifiers (OTAs). The CF element has been created by the CCCII cell of the chip. For the CCCII working as a CF, the X terminal is used as a current input and the Y terminal is grounded. The relation

TABLE 1. Setting of the control of the CM FO integrator depending on the desired order.

Order α [-]	0.1	0.3	0.5	0.7	0.9
g_{m1} [mS]	0.5	0	0	0	0
g_{m2} [mS]	0	0.5	0	0	0
g_{m3} [mS]	0	0	0.5	0	0
g_{m4} [mS]	0	0	0	0.5	0
g_{m5} [mS]	0	0	0	0	0.5

of this element is given as $I_{OUT\pm} = \pm I_{IN}$. As for the OTA elements, the CMOS multiplication units have been used. This particular implementation of the OTA element provides the electronic control of its transconductance by a DC control voltage (V_{SET_gm}). The behavior of the OTA can be described as $I_{OUT\pm} = \pm g_m \cdot (V_{IN+} - V_{IN-})$.

The number of OTAs is depending on how many orders we want to obtain, the required variety of the desired orders, respectively. For the design introduced in this paper, we consider the orders 0.1, 0.3, 0.5, 0.7, and 0.9 (five orders). This requires five branches of the proposed integrator and thus five OTAs. We consider such variety of possible orders sufficient for our needs. If a higher variety of available orders is required, the number of branches can be increased (theoretically indefinitely according to the required variety). For the integrator providing five orders, it means 1 additional output for the CF element, nonetheless for the on–chip implementation this causes no significant issue (for the used implementation it means 4 additional transistors of the internal topology of CCCII cell). Each branch also contains an RC structure of specific values corresponding with the particular order. The resulting order of the integrator is depending on the setting of control of the OTAs. Each order is available by setting a specific OTA (other OTAs are set to zero). For example, if we want the order of the integrator to be equal to 0.3, OTA$_2$ is used and the control of the remaining OTAs is set to zero. That way, we will obtain the response of the desired order at the output of the integrator with other branches of remaining orders not being used at the moment. Thus, the control of the resulting order is simple (either being switched on or off). In such case, it would be easier to use simple electronically controllable switches rather than comparably complex CMOS structure of the OTAs, however, using the OTAs offers a possibility of additional electronic adjustment of the integrator parameters (possibility of the gain adjustment in this particular case). Also, as the used multiplication unit can work in all four quadrants, it can offer a possibility to invert the polarity of the output response. The specific setting of the integrator, in correspondence with the desired order, is presented in Table 1. The default used value of the transconductance when the OTA is set was chosen to be 0.5 mS.

The transfer function of the integrator from Fig. 1 is expressed as:

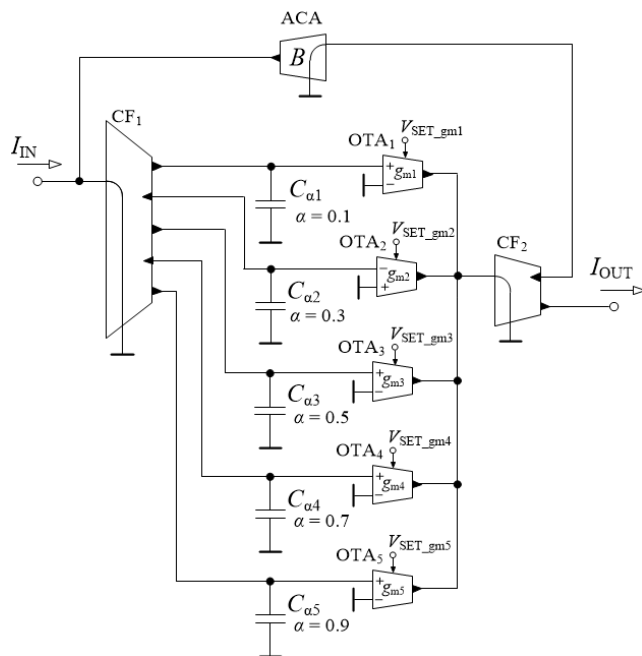$$\frac{I_{OUT}}{I_{IN}} = \frac{g_{mi}}{s^\alpha C_{\alpha i}} \tag{1}$$

FIGURE 2. Modified structure of the CM integrator allowing to electronically change between lossy and lossless behavior.

where g_{mi} and $C_{\alpha i}$ denote the specific transconductance and FO capacitance depending on which order is currently used thus, $i = \{1, 2, 3, 4, 5\}$.

From (1), it is evident that the integrator is lossless. Fig. 2 shows a possible modification of the proposed CM integrator from Fig. 1. This modification consists of one additional CF (CF$_2$) and one adjustable current amplifier (ACA) added into the structure of the proposed integrator. The ACA element is described by the equation $I_{OUT\pm} = \pm B \cdot I_{IN}$, where B is the current gain of this element. The advantage of this modification is that we can easily switch between the integrator behaving as lossless or lossy by electronic means (current gain B controlled either by DC voltage or DC current depending on specific implementation of the ACA). This means two more active elements in the structure, nonetheless, the presence of the CF with multiple outputs (more than two) at the output of the integrator is desirable as the design of CM circuits, frequency filters in particular, often requires the necessity of multiple outputs of the building block (integrator) for feedback loops. The CF at the output also provides an impedance separation. The transfer function of the modified integrator is given by:

$$\frac{I_{OUT}}{I_{IN}} = \frac{g_{mi}}{s^\alpha C_{\alpha i} + g_{mi} B} \tag{2}$$

From (2), it can be seen that, the integrator behaves as lossless for $B = 0$, when the integrator follows the equation (1), or lossy for $B = 1$.

III. SIMULATION AND EXPERIMENTAL RESULTS OF THE PROPOSED CM FO INTEGRATOR

The simulation results were carried out in Cadence IC6 (spectre) software using the simulation model in

CMOS 0.35 μm I3T25 ON Semiconductor technology. The experimental measurements were performed with help of a network analyzer Agilent 4395A and simple V–I/I–V converters based around commercially available OPA860 device [51]. The measurement arrangement using a testing board, which can include up to four chips, is displayed in Fig. 3 (the board also includes the converters and trimmers to set bias currents).
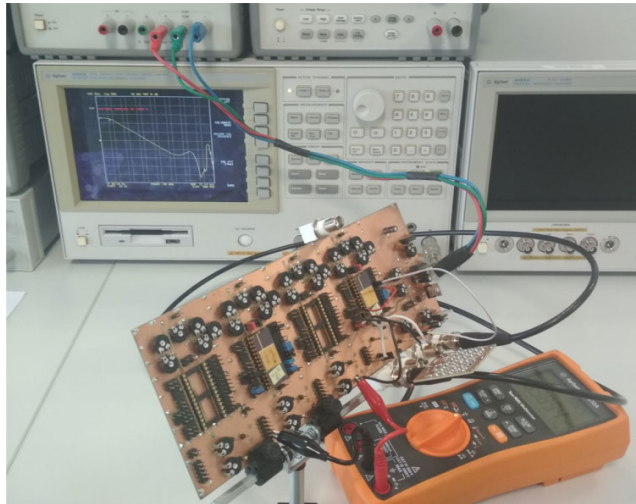

FIGURE 3. Arrangement of the measuring workplace.

RC structures of required orders have been implemented for the purposes of simulations and experimental measurements. A 5th–order Foster I type RC topology shown in Fig. 4 has been used. The values of the individual parts of the RC structures depending on the order were calculated using the Oustaloup approximation [52] in Matlab software for the central frequency f_C = 10 kHz. The particular values are summarized in Table 2.

The values of transconductances of individual OTA elements in the integrator structure are either set to zero or 0.5 mS as already mentioned in the previous section. The value 0.5 mS corresponds with the value V_{SET_gm} of 0.26 V in simulations and 0.39 V in case of the experimental measurements due to differences between the simulated and measured transconductance values in dependence on the control voltage which was $g_m \approx 2 \cdot V_{SET\_gm}$ [mS] for the simulations and $g_m \approx 1.3 \cdot V_{SET\_gm}$ [mS] for the implemented chip (standardly expected deviations fitting process corners, voltage and temperature variations) [50]. The supply voltage of the chip is ± 1.65 V and the supply voltage of the chips (OPA860) used for the converters is ± 5 V. The power consumption of one CCCII is 16.8 mW, and it is 7.8 mW in case of one multiplication unit. Therefore, the power consumption of the topology in Fig. 1 is 55.8 mW and 72.6 mW + the power consumption of the ACA depending on its implementation for the modified circuit in Fig. 2.

Fig. 5 shows a comparison of the theoretical expectations (black dashed lines) and simulation results (colored lines)
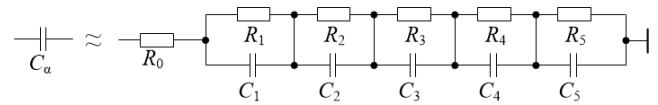

FIGURE 4. Used RC topology of the 5th–order Foster I type.

TABLE 2. Values of the individual parts within the RC structure in correlation with the desired order.

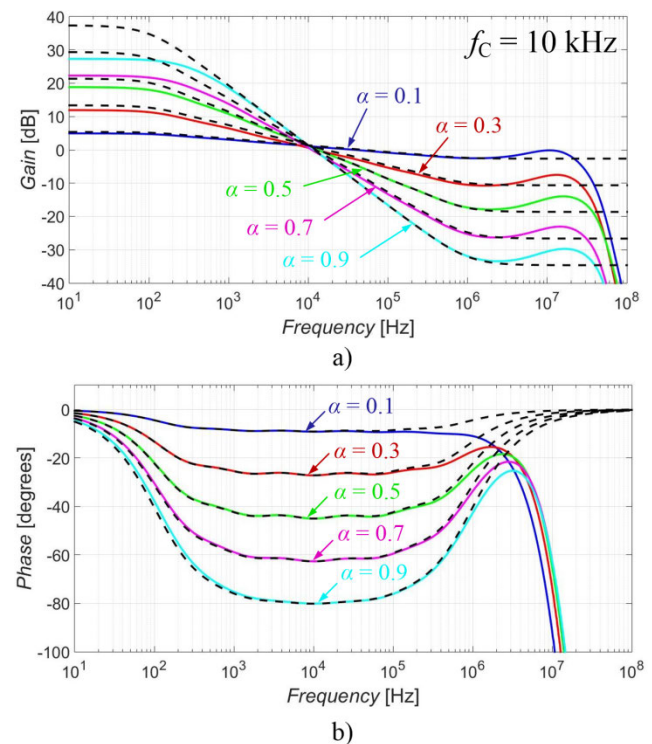| Order α [-]	0.1	0.3	0.5	0.7	0.9
R_0 [Ω]	1476.8	587.9	234.1	93.2	37.1
R_1 [Ω]	285.6	365.1	241.5	113.9	27.5
R_2 [Ω]	354.2	685.6	676.1	470.7	166.8
R_3 [Ω]	428.1	1208.0	1735.2	1759.5	909.1
R_4 [Ω]	517.7	2143.6	4546.3	6872.6	5374.7
R_5 [Ω]	647.1	4327.5	15972.0	49481.2	141151.4
C_1 [nF]	1.54	1.44	2.62	6.69	33.3
C_2 [nF]	7.81	4.85	5.91	10.2	34.6
C_3 [nF]	40.8	17.4	14.5	17.2	40.1
C_4 [nF]	212.7	61.8	35.0	27.8	42.8
C_5 [nF]	1073.6	193.0	62.9	24.4	10.3

a)

b)

FIGURE 5. Magnitude (a)) and phase (b)) characteristics of the proposed integrator for used orders (0.1, 0.3, 0.5, 0.7 and 0.9): theoretical expectations (black dashed lines), simulation results (colored lines).

of the magnitude and phase characteristics of the proposed integrator for the electronic adjustment of the order (for orders 0.1, 0.3, 0.5, 0.7 and 0.9). The electronic adjustment of the order is given by Table 1. The largest differences between the theoretical expectations and simulation results can be seen mainly at lower frequencies, where the magnitude characteristics of simulation results do not reach the same

gain level as the theoretical expectations which is caused by the real characteristics of the output impedances of the active elements, limitations of the linear behavior of the chip in relation to the values of used transconductances and by the DC offset being too high for used gain. Similarly, the differences between the theoretical expectations and simulation results at higher frequencies are caused by the influence of the real characteristics of the input impedances and bandwidth limitation of the chip (up to about 40 MHz). For higher orders, the difference between the theoretical expectations and the simulation results at lower frequencies increases more significantly than for lower orders. Therefore, the design (for given implementation) is more suitable for frequencies above about 300 Hz. Nonetheless, despite of these expected differences, the results confirm the intended function of the proposed circuit and agreement with the theoretical presumptions in general.
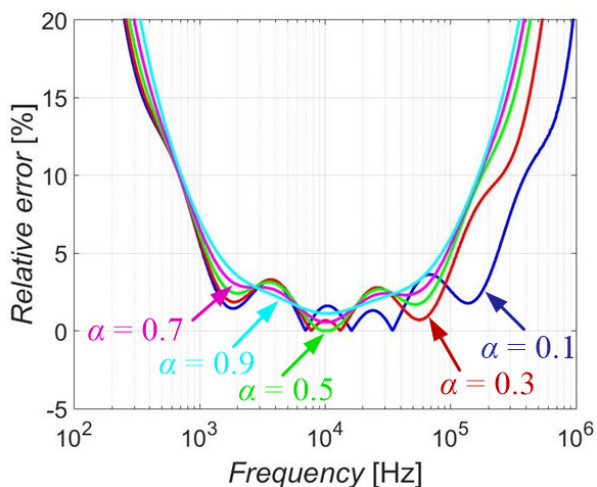

FIGURE 6. Relative error of the phase characteristics obtained from simulation compared to the theoretical phase shift of given order.

In order to evaluate the performance of the proposed integrator, evaluate the accuracy of the resulting order of the integrator and its bandwidth, where the FO approximation is valid, a relative error of the phase characteristics across the frequency was carried out (Fig. 6). The error is expressed in percentage as a deviation of the value of the phase obtained from the simulations compared to the theoretical (ideal) value of phase shift for given order (e. g. $-9°$, $-27°$, $-45°$, $-63°$ and $-81°$ (constant across all frequencies) for orders 0.1, 0,3, 0,5, 0,7 and 0.9). The usable bandwidth (f_{min}, f_{max}) of given order, established for a frequency band with a relative error under 10%, is summarized in Table 3. From the table, it can be seen that the operational bandwidth, where the FO approximation is valid (for the used 5th–order RC structure), is above 2 decades in all cases. Note that if a wider operational bandwidth is required, an RC structure of higher order can be easily designed to cover these requirements.

As mentioned earlier, the presence of OTAs in the individual branches of the proposed circuit offers a possibility of

TABLE 3. Comparison of operational bandwidths for used orders where the relative error is under 10% in case of simulation results.

α [-]	f_{min} [HZ]	f_{max} [kHz]	Bandwidth
0.1	684	394	> 2 decades
0.3	684	254	> 2 decades
0.5	684	176	> 2 decades
0.7	692	170	> 2 decades
0.9	716	166	> 2 decades

the electronic control of the gain adjustment by changing the values of the transconductances. This ability has been tested for five different settings of the transconductance when the order of the integrator is set to 0.5. The chosen values of the transconductance are 0.7 mS, 0.6 mS, 0.5 mS, 0.4 mS and 0.3 mS corresponding with the control voltages of 0.36 V, 0.31 V, 0.26 V, 0.21 V and 0.15 V. The simulation results compared with the theoretical expectations are depicted in Fig. 7. The results in the graph show that the gain of the integrator can be adjusted by electronic means while the order stays unchanged as suggested by phase characteristics which are practically identical.
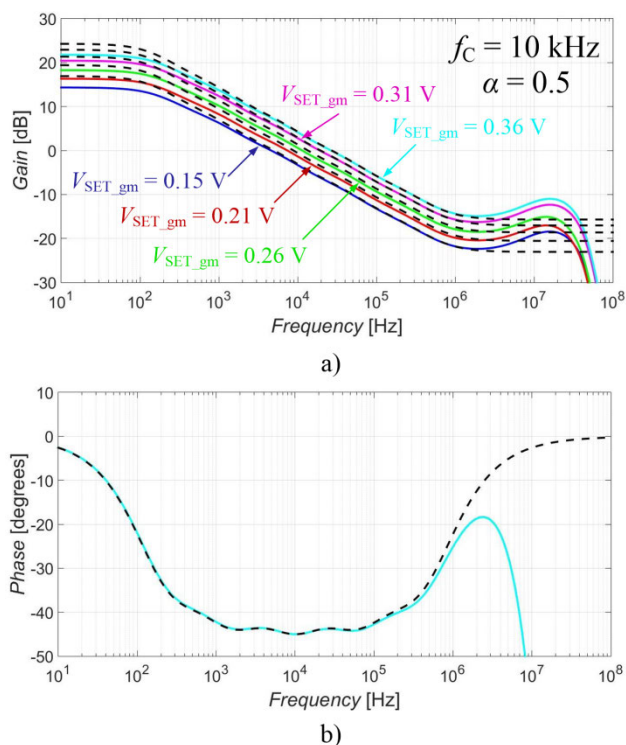

a)

b)

FIGURE 7. Demonstration of the electronic control of the gain adjustment of the proposed integrator for order 0.5: theoretical expectations (black dashed lines), simulation results (colored lines).

Simulation results of a sinusoidal wave response (see Fig. 8) of the proposed integrator for used fractional orders has been carried out in order to analyze the behavior of the integrator in the time domain. The input excitation signal (black line) has the following characteristics: amplitude is
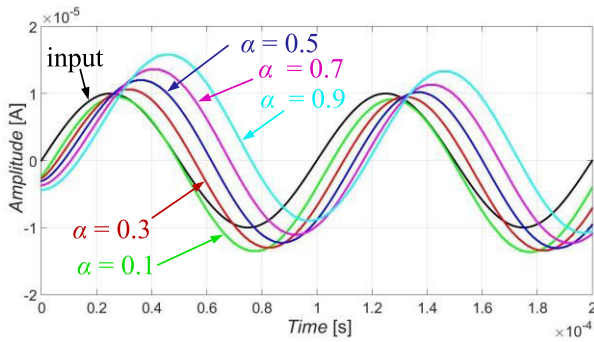
FIGURE 8. Transient responses to a sinusoidal wave input signal for used orders in case of simulation results.

equal to 10 µA (20 µA peak–to–peak), frequency has been set to 10 kHz (corresponding with the central frequency of the operational bandwidth of the integrator). The output responses (colored lines) for used orders (0.1, 0.3, 0.5, 0.7 and 0.9) show the phase shifts of −8.5°, −26.2°, −43.3°, −60.4° and 76.9°.
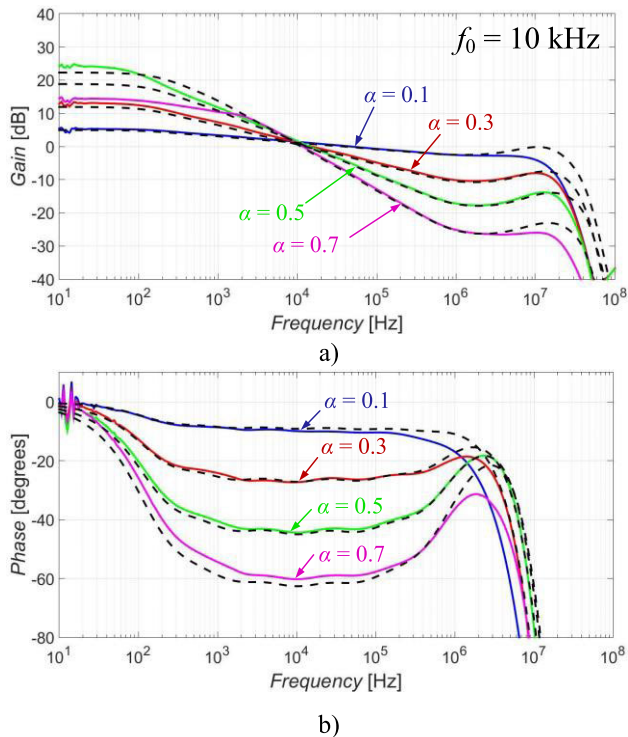

a)

b)

FIGURE 9. Magnitude (a)) and phase (b)) characteristics of the proposed integrator for used orders (0.1, 0.3, 0.5, 0.7): simulation results (black dashed lines), experimental measurements (colored lines).

Fig. 9 compares the simulation results (black dashed lines) and experimental measurements (colored lines) of the magnitude and phase characteristics for used orders. The experimental results further support the design. In case of the experimental measurements, the integrator for order 0.9 already did not work properly due to the mutual interaction of the impedance of the RC structure and real/parasitic

characteristics of the output impedances of used active elements. Therefore, the experimental results for order 0.9 are not included as they do not provide any useful contribution. This issue could be solved by the recalculation of the RC structure with different values of capacitors resulting in more favorable values of resistors being used.

A relative error of the phase characteristics obtained from the experimental measurements compared to the theoretical (ideal) value of phase shift for given order (−9°, −27°, −45°, −63° and −81° for orders 0.1, 0,3, 0,5, 0.7 and 0.9) is depicted in Fig. 10. As the characteristics of measurements for order 0.9 are not available, the error is not presented in Fig. 10 and in Table 4, where the information about usable bandwidth is given. Comparing the bandwidths obtained from the simulations and experimental measurements, the implemented integrator exhibits narrower bandwidths as the effect of real/parasitic impedances is typically more significant in case of the measurement.
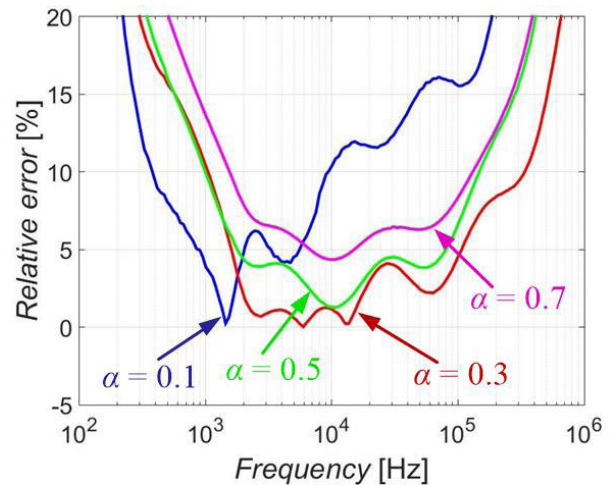

FIGURE 10. Relative error of the phase characteristics obtained from the experimental measurements compared to the theoretical phase shift of given order.

TABLE 4. Comparison of operational bandwidths for used orders where the relative error is under 10% in case of experimental measurements.

α [-]	f_{min} [HZ]	f_{max} [kHz]	Bandwidth
0.1	369	9.5	< 2 decades
0.3	1070	330	> 2 decades
0.5	1000	144	> 2 decades
0.7	1530	128	< 2 decades
0.9	-	-	-

The demonstration of the electronic control of the gain adjustment (when α is set to 0.5) by changing the values of the transconductances comparing the simulation results and the experimental measurements is shown in Fig. 11. The control voltages for selected values of transconductances (0.7 mS, 0.6 mS, 0.5 mS, 0.4 mS and 0.3 mS) in case of the

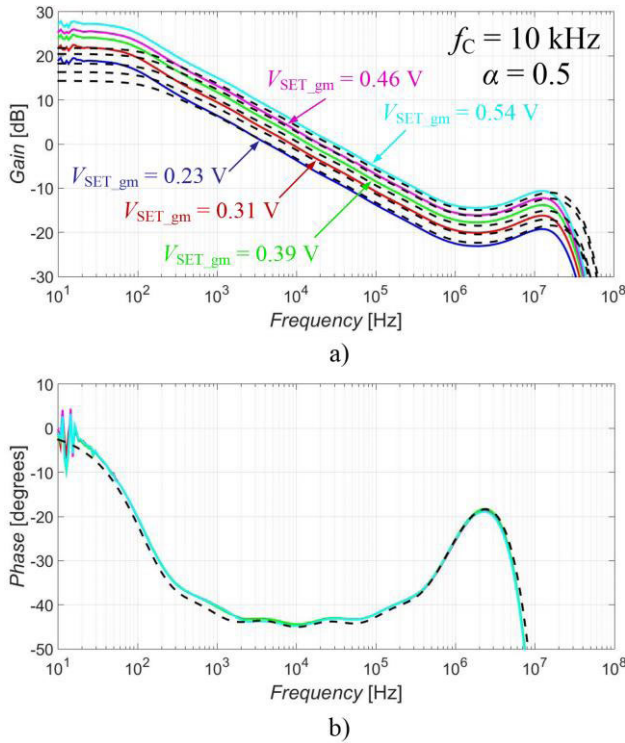experimental measurements are 0.54 V, 0.46 V, 0.39 V, 0.31 V and 0.23 V.

FIGURE 11. Demonstration of the electronic control of the gain adjustment of the proposed integrator for order 0.5: simulation results (black dashed lines), experimental measurements (colored lines).
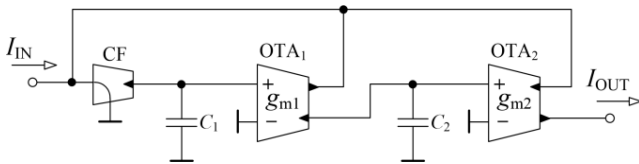

FIGURE 12. Topology of a CM second–order low–pass FLF filter used for demonstrational purposes.

IV. APPLICATION EXAMPLE OF THE PROPOSED INTEGRATOR

The integrator has been implemented into a structure of a frequency filter (in order to provide fractional–order characteristics) as a possible utilization of the introduced design. A structure used for this matter is a simple current–mode second–order low–pass filter based on Follow–the–Leader–Feedback (FLF) topology (shown in Fig. 12). It consists of one CF, two OTAs and two grounded capacitors. The transfer function for this topology is given as:

$$K(s) = \frac{I_{OUT}}{I_{IN}} = \frac{g_{m1}g_{m2}}{s^2 C_1 C_2 + s C_2 g_{m1} + g_{m1}g_{m2}} \quad (3)$$

For the filter to provide FO characteristics, OTA$_2$ and C_2 were replaced by the proposed CM FO integrator as shown
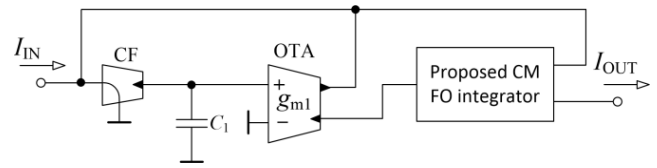

FIGURE 13. Modified filter from Fig. 12 with the proposed CM FO integrator behaving as a $1 + \alpha$ low–pass filter.

in Fig 13. Thus, the modified topology behaves as a $1 + \alpha$ low–pass filter. The transfer function from (3) turns into:

$$K(s) = \frac{I_{OUT}}{I_{IN}} = \frac{g_{m1}g_{m2}}{s^{1+\alpha}C_1 C_{2\alpha} + s^\alpha C_{2\alpha}g_{m1} + g_{m1}g_{m2}} \quad (4)$$

As the proposed integrator offers only one output (not considering the modification discussed at the end of section II), the additional required outputs were obtained by the addition of a CCCII operating as a CF at the output of the integrator.

In order for the transition between of the output response of the filter having Butterworth characteristics, coefficients k need to be applied onto the general FO low-pass function as:

$$K_{1+\alpha}^{LP}(s) = \frac{k_1}{s^\alpha(s + k_2) + k_3} \quad (5)$$

where $k_1 = 1$, $k_2 = 1.008\alpha^2 + 0.2867\alpha + 0.2366$ and $k_3 = 0.2171\alpha + 0.7914$.

The function of such modified filter has been tested by cadence simulations and compared to the theoretical expectations. The value of C_1 has been set to 10 nF. Together with chosen pole frequency f_0 equal to 5 kHz, the values of transconductances g_{m1} of the filter and g_{m2} (substituted by the transconductance of the integrator) have to be calculated by the comparison of (4) and (5) in respect to coefficients k depending on the value of α. The values of transconductances for given α are stated in Table 5. The characteristics (magnitude and phase) of the filter for used orders (0.1, 0,3, 0,5, 0,7 and 0.9) are presented in Fig. 14, where black dashed lines stand for the theoretical results and colored lines represent the simulation results. It can be seen that the filter is behaving as expected – providing different fractional orders based on the setting of the proposed integrator. The simulation results show good agreement with the theory up to frequency of about 2 MHz, where the influence of the real characteristics of used active elements becomes more pronounced.

TABLE 5. Values of transconductances in relation to selected value of alpha.

Order α [-]	0.1	0.3	0.5	0.7	0.9
g_{m1} [mS]	0.09	0.13	0.20	0.29	0.41
g_{m2} [mS]	0.63	0.44	0.30	0.22	0.16

The ability of the electronic control of the gain adjustment of the proposed integrator can be beneficial in case of the control of the pole frequency of the filter. The pole frequency
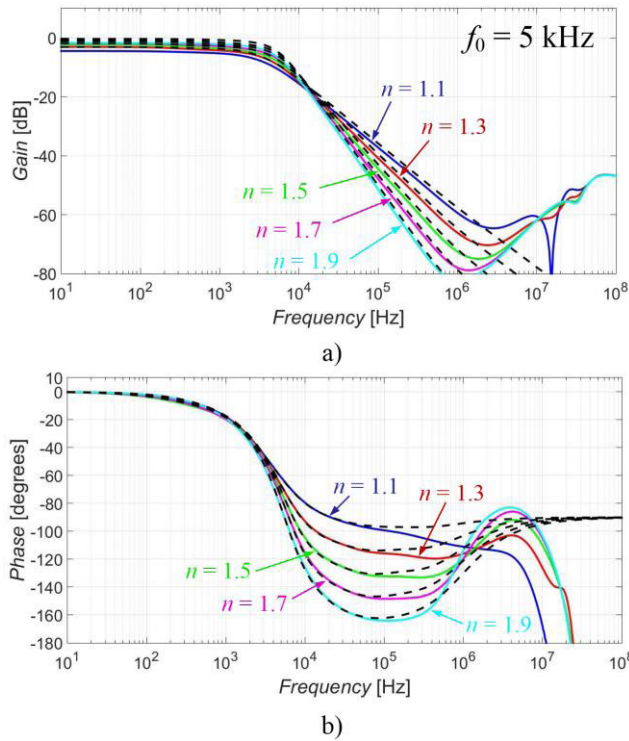
FIGURE 14. Magnitude (a)) and phase (b)) characteristics of the $1 + \alpha$ filter for used orders (0.1, 0.3, 0.5, 0.7 and 0.9): theoretical expectations (black dashed lines), simulation results (colored lines).

of the filter can be controlled by adjusting the value of given transconductance g_{mi} of the integrator (substituting g_{m2} of the filter) together with transconductance g_{m1} of the filter. The ability of the electronic control of the pole frequency has been tested for three settings (specified in Table 6). The results are shown in Fig 15 for theoretical expectations (black dashed lines) and simulations (colored lines) when the order of the filter was set to 1.5 ($\alpha = 0.5$). From the graphs, it can be seen that the order and quality factor of the output responses remain unaffected when changing the pole frequency. Furthermore, the simulation results are corresponding well with the theoretical expectations and support the fact that the available electronic control of the gain adjustment of the proposed integrator can find its application in circuits.

TABLE 6. Values of transconductances for tested pole frequencies.

f_0 [kHz]	2.5	5	10
g_{m1} [mS]	0.1	0.2	0.4
g_{m2} [mS]	0,15	0.3	0.6

V. COMPARISON AND DISCUSSION

Table 7 provides a summary of recently introduced FO integrators/differentiators and their features. Some papers ([40]–[42]) contain the design of both FO integrator and
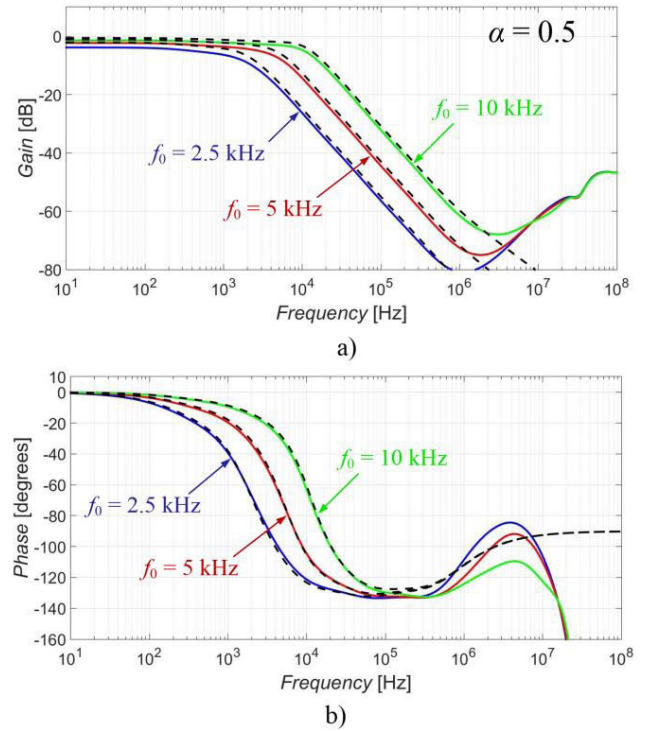

FIGURE 15. Illustration of the electronic control of the pole frequency of the filter when the order is 1.5 ($\alpha = 0.5$).

differentiator as separate circuits while papers [44], [45] and [47] propose one topology which can offer the FO integration/derivation function. Circuits in [40]–[42] use the RC structures for their function while topologies in [43]–[49] are based on the approximation of Laplacian operator of the fractional order. The circuits proposed in [41]–[43], [48] and [49] operate in the voltage mode, circuits in [44]–[47] operate in the current mode and paper [40] offers designs working in both modes. Note that the designs based on the RC structure [40]–[42] typically do not offer the electronic control of the resulting fractional order. The RC structure has to be mechanically replaced for the integrator/differentiator design in order to provide a different fractional order which is the most significant disadvantage of this approach. On the other hand, the circuits [43]–[49] based on the approximation standardly utilize the electronic control of the order (and other parameters in specific cases). Paper [43] is an exception as the introduced circuit uses passive parts of specific values in order to obtain the FO approximation rather than using electronically controllable active elements and thus, this paper does not offer any electronic control. The disadvantage of topologies based on the approximation consists in the usually complex control/adjustment because multiple quite specific and precise values of the control voltages/currents are required for the accurate approximation (see papers [44]–[49] for exact values control voltages/currents). Thus, specific values of the control voltages/currents which might be difficult to obtain (e.g. very low values of control voltage in hundredths and thousandths of volts for α closing zero or one).

TABLE 7. Comparative summary of recently introduced fractional–order integrators/differentiators.

Reference number	Year of publication	Proposed circuitry (number of presented circuits)	Type of realization	Available mode(s)	Possibility to electronically control f_C/gain/order	Type of control	Available bandwidth	Simulated/measured	Notes
[40]	2019	Int(2), Diff(2)	RC	CM/VM	No/Yes/No	Simple	3 decades	Yes/No	-
[41]	2020	Int(1), Diff(1)	RC	VM	No/Yes/No	Simple	6 decades	Yes/No	1
[42]	2020	Int(1), Diff(1)	RC	VM	No/Yes/No	Simple	6 decades	Yes/Yes	1
[43]	2015	Int(2)	Approx.	VM	No/No/No	-	< 2 decades	Yes/No	-
[44]	1019	Int/Diff(1)	Approx.	CM	Yes/No/Yes	Complex	3 decades	Yes/No	2
[45]	2018	Int/Diff(1)	Approx.	CM	Yes/No/Yes	Complex	< 2 decades	Yes/No	2
[46]	2020	Int(2)	Approx.	CM	Yes/No/Yes	Complex	2/3 decades	Yes/Yes	2
[47]	2015	Int/Diff(1)	Approx.	CM	Yes/No/Yes	Complex	< 2 decades	Yes/No	2
[48]	2017	Int(1)	Approx.	VM	Yes/No/Yes	Complex	< 2 decades	Yes/No	2
[49]	2015	Int(1)	Approx.	VM	Yes/No/Yes	Complex	< 2 decades	Yes/No	2
This work	-	Int(1)	RC	CM	No/Yes/Yes	Simple	2 decades	Yes/Yes	-

List of previously unexplained abbreviations used in Table VII:
Int – integrator, Diff – differentiator, RC - RC ladder network, Approx. – circuit based on the approximation of Laplacian operator of fractional order

Notes:
[1] presented topology is using the RC structure of the 10th–order to provide the bandwidth of 6 decades,
[2] the electronic control of the gain adjustment is theoretically possible but not presented

We also usually require rather specific values of the control voltages/currents where the change of units of mili-volts or units of micro-amperes can cause a significant difference which might lead to an inaccuracy of the FO approximation.

The design proposed in this paper is based on RC structures, but in comparison to other RC structure based integrators/differentiators, it offers the electronic control of the order (and the electronic control of the gain). Compared to the circuits based on the approximation, the presented design brings a simple control of the resulting fractional order as it depends on whether given branch is on or off regardless of the value of the control (control voltage in this case) as described in sections II. The value of the control only determines the gain level of the resulting output response.

Comparing the circuitry introduced in this paper with other designs, the proposed design brings following:

- It is based on RC structures, but in comparison to other RC structure based designs [40]–[42] it offers the electronic control of its order.
- Unlike circuits in [40]–[42], the mechanical replacement of the RC structure in order to obtain a different fractional order is not necessary.
- In comparison to designs [43]–[49], our solution provides a simple control of its order where we do not require multiple specific and accurate values of control voltages/currents.
- Available bandwidth of the proposed solution is 2 decades where only [40] and [44] offer better results. (Papers 41] and [42] use a RC structure of the 10th–order and thus their available bandwidth cannot be directly compared with the proposed solutions)
- The design proposed in this paper is supported not only by simulations but also by experimental measurement. This only applies for papers [42] and [46].

VI. CONCLUSION

The simulation and experimental results prove the function of the proposed CM FO integrator. The results are in good agreement with the theoretical expectations except for the order 0.9 in case of the experimental measurements (a possible solution of this issue is discuses in section III). The performance of the proposed integrator for different orders is summed in Table 3 for the simulations and Table 4 for the measurements. The integrator can offer the electronic control of the order unlike other RC structure based solutions of the FO integrators. Furthermore, the control of the order is simple and does not require specific and very accurate values of sets of many parameters in comparison to the designs based on the approximation of the FO Laplacian operator. Thus, the described research offers a different approach avoiding the disadvantages of above mentioned methods. The integrator also introduces the additional feature of the electronic control of the gain level/gain adjustment as demonstrated in Figs. 7 and 11. A possible utilization of the proposed FO integrator in a topology of a standard second–order frequency filter for obtainment of a $1+\alpha$ filter is tested. Obtained results (Fig. 14 and 15) support the intended usage of the proposed integrator in the design of further FO applications.

REFERENCES

[1] T. J. Freeborn, "A survey of fractional-order circuit models for biology and biomedicine," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 3, no. 3, pp. 416–424, Sep. 2013, doi: 10.1109/JETCAS.2013.2265797.

[2] S. Das and K. Maharatna, "Fractional dynamical model for the generation of ECG like signals from filtered coupled Van-der Pol oscillators," *Comput. Methods Programs Biomed.*, vol. 112, pp. 490–507, Dec. 2013, doi: 10.1016/j.cmpb.2013.08.012.

[3] V. De Santis, V. Martynyuk, A. Lampasi, M. Fedula, and M. D. Ortigueira, "Fractional-order circuit models of the human body impedance for compliance tests against contact currents," *AEU Int. J. Electron. Commun.*, vol. 78, pp. 238–244, Aug. 2017, doi: 10.1016/j.aeue.2017.04.035.

[4] T. J. Freeborn, B. Maundy, and A. S. Elwakil, "Extracting the parameters of the double-dispersion Cole bioimpedance model from magnitude response measurements," *Med. Biol. Eng. Comput.*, vol. 52, no. 9, pp. 58–749, 2014, doi: 10.1007/s11517-014-1175-5.

[5] T. Abuaisha and J. Kertzscher, "Fractional-order modelling and parameter identification of electrical coils," *Fractional Calculus Appl. Anal.*, vol. 22, no. 1, pp. 193–216, Feb. 2019, doi: 10.1515/fca-2019-0013.

[6] T. J. Freeborn, A. S. Elwakil, and B. Maundy, "Variability of Cole-model bioimpedance parameters using magnitude-only measurements of apples from a two-electrode configuration," *Int. J. Food Properties*, vol. 20, no. 1, pp. 507–519, 2017, doi: 10.1080/10942912.2017.1300810.

[7] C. Flores, J. Muñoz, C. A. Monje, V. Milanés, and X.-Y. Lu, "Iso-damping fractional-order control for robust automated car-following," *J. Adv. Res.*, vol. 25, pp. 181–189, Sep. 2020, doi: 10.1016/j.jare.2020.05.013.

[8] F. Khateb, D. Kubánek, G. Tsirimokou, and C. Psychalinos, "Fractional-order filters based on low-voltage DDCCs," *Microelectron. J.*, vol. 50, pp. 50–59, Apr. 2016, doi: 10.1016/j.mejo.2016.02.002.

[9] R. Verma, N. Pandey, and R. Pandey, "CFOA based low pass and high pass fractional step filter realizations," *AEU Int. J. Electron. Commun.*, vol. 99, pp. 161–176, Feb. 2019, doi: 10.1016/j.aeue.2018.11.032.

[10] B. Maundy, A. S. Elwakil, and T. J. Freeborn, "On the practical realization of higher-order filters with fractional stepping," *Signal Process.*, vol. 91, no. 3, pp. 484–491, 2011, doi: 10.1016/j.sigpro.2010.06.018.

[11] S. K. Mishra, M. Gupta, and D. K. Upadhyay, "Active realization of fractional order Butterworth lowpass filter using DVCC," *J. King Saud Univ. Eng. Sci.*, vol. 32, no. 2, pp. 158–165, Feb. 2020, doi: 10.1016/j.jksues.2018.11.005.

[12] G. Tsirimokou, R. Sotner, J. Jerabek, J. Koton, and C. Psychalinos, "Programmable analog array of fractional-order filters with CFOAs," in *Proc. 40th Int. Conf. Telecommun. Signal Process. (TSP)*, Barcelona, Spain, Jul. 2017, pp. 706–709, doi: 10.1109/TSP.2017.8076079.

[13] D. V. Kamath, S. Navya, and N. Soubhagyaseetha, "Fractional order OTA-C current-mode all-pass filter fractional order OTA-C current-mode all-pass filter," in *Proc. 2nd Int. Conf. Inventive Commun. Comput. Technol. (ICICCT)*, Coimbatore, India, Apr. 2018, pp. 383–387, doi: 10.1109/ICICCT.2018.8473097.

[14] S. K. Mishra, M. Gupta, and D. K. Upadhyay, "A low-power compact DDCC based fractional-order filter," in *Proc. 2nd Int. Conf. Power, Energy Environ., Towards Smart Technol. (ICEPE)*, Jun. 2018, pp. 1–6, doi: 10.1109/EPETSG.2018.8658517.

[15] L. Langhammer, R. Sotner, J. Dvorak, J. Jerabek, and P. A. Ushakov, "Novel reconnection-less reconfigurable filter design based on unknown nodal voltages method and its fractional-order counterpart," *Elektronika Elektrotechnika*, vol. 25, no. 3, pp. 34–38, Jun. 2019, doi: 10.5755/j01.eie.25.3.23673.

[16] L. A. Said, S. M. Ismail, A. G. Radwan, A. H. Madian, M. F. A. El-Yazeed, and A. M. Soliman, "On the optimization of fractional order low-pass filters," *Circuits, Syst., Signal Process.*, vol. 35, no. 6, pp. 2017–2039, 2016, doi: 10.1007/s00034-016-0258-y.

[17] R. Verma, N. Pandey, and R. Pandey, "Electronically tunable fractional order filter," *Arabian J. Sci. Eng.*, vol. 42, no. 8, pp. 3409–3422, Aug. 2017, doi: 10.1007/s13369-017-2500-8.

[18] L. A. Said, A. G. Radwan, A. H. Madian, and A. M. Soliman, "Two-port two impedances fractional order oscillators," *Microelectron. J.*, vol. 55, pp. 40–52, Sep. 2016, doi: 10.1016/j.mejo.2016.06.003.

[19] A. S. Elwakil, A. Agambayev, A. Allagui, and K. N. Salama, "Experimental demonstration of fractional-order oscillators of orders 2.6 and 2.7," *Chaos, Solitons Fractals*, vol. 96, pp. 160–164, Mar. 2017, doi: 10.1016/j.chaos.2017.01.017.

[20] G. Tsirimokou, C. Psychalinos, A. Elwakil, and B. J. Maundy, "Analysis and experimental verification of a fractional-order Hartley oscillator," in *Proc. Eur. Conf. Circuit Theory Design (ECCTD)*, Catania, Italy, Sep. 2017, pp. 1–4, doi: 10.1109/ECCTD.2017.8093312.

[21] R. Sotner, J. Jerabek, L. Langhammer, A. Kartci, N. Herencsar, and B. Metin, "Practical design of fractional-order resonator for application in the multiphase oscillator," in *Proc. 27th IEEE Int. Conf. Electron., Circuits Syst. (ICECS)*, Glasgow, U.K., Nov. 2020, pp. 1–4, doi: 10.1109/ICECS49266.2020.9294799.

[22] L. A. Said, O. Elwy, A. H. Madian, A. G. Radwan, and A. M. Soliman, "Stability analysis of fractional-order colpitts oscillators," *Anal. Integr. Circuits Signal Process.*, vol. 101, no. 2, pp. 267–279, Nov. 2019, doi: 10.1007/s10470-019-01501-2.

[23] M. E. Fouda, A. Soltan, A. G. Radwan, and A. M. Soliman, "Fractional-order multi-phase oscillators design and analysis suitable for higher-order PSK applications," *Analog Integr. Circuits Signal Process.*, vol. 87, no. 2, pp. 301–312, 2016, doi: 10.1007/s10470-016-0716-2.

[24] C. Vastarouchas, G. Tsirimokou, T. J. Freeborn, and C. Psychalinos, "Emulation of an electrical-analogue of a fractional-order human respiratory mechanical impedance model using OTA topologies," *AEU Int. J. Electron. Commun.*, vol. 78, pp. 201–208, Aug. 2017, doi: 10.1016/j.aeue.2017.03.021.

[25] W. Bauer, J. Baranowski, S. Kapoulea, and C. Psychalinos, "Digital and analog design of fractional PD controller for a servo system," in *Proc. 24th Int. Conf. Methods Models Automat. Robot. (MMAR)*, Miedzyzdroje, Poland, Aug. 2019, pp. 472–477, doi: 10.1109/MMAR.2019.8864626.

[26] M. S. Tavazoei, M. Tavakoli-Kakhki, and F. Bizzarri, "Nonlinear fractional-order circuits and systems: Motivation, a brief overview, and some future directions," *IEEE Open J. Circuits Syst.*, vol. 1, pp. 220–232, 2020, doi: 10.1109/OJCAS.2020.3029254.

[27] R. Sotner, L. Langhammer, J. Jerabek, P. A. Ushakov, and T. Dostal, "Fractional-order phase shifters with constant magnitude frequency responses," *Elektronika Elektrotechnika*, vol. 25, no. 5, pp. 25–30, Oct. 2019, doi: 10.5755/j01.eie.25.5.24352.

[28] G. Tsirimokou, C. Psychalinos, A. S. Elwakil, and K. N. Salama, "Electronically tunable fully integrated fractional-order resonator," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 2, pp. 166–170, Feb. 2018, doi: 10.1109/TCSII.2017.2684710.

[29] A. Soltan, L. Xia, A. Jackson, G. Chester, and P. Degenaar, "Fractional order PID system for suppressing epileptic activities," in *Proc. IEEE Int. Conf. Appl. Syst. Invention (ICASI)*, Chiba, Japan, Apr. 2018, pp. 338–341.

[30] A. S. Elwakil, "Fractional-order circuits and systems: An emerging interdisciplinary research area," *IEEE Circuits Syst. Mag.*, vol. 10, no. 4, pp. 40–50, Nov. 2010, doi: 10.1109/MCAS.2010.938637.

[31] M. C. Tripathy, D. Mondal, K. Biswas, and S. Sen, "Experimental studies on realization of fractional inductors and fractional-order bandpass filters," *Int. J. Circuit Theory Appl.*, vol. 43, no. 9, pp. 1183–1196, 2015, doi: 10.1002/cta.2004.

[32] M. S. Krishna, S. Das, K. Biswas, and B. Goswami, "Fabrication of a fractional order capacitor with desired specifications: A study on process identification and characterization," *IEEE Trans. Electron Devices*, vol. 58, no. 11, pp. 4067–4073, Nov. 2011, doi: 10.1109/TED.2011.2166763.

[33] T. C. Haba, G. Ablart, T. Camps, and F. Olivie, "Influence of the electrical parameters on the input impedance of a fractal structure realised on silicon," *Chaos, Solitons Fractals*, vol. 24, no. 2, pp. 479–490, 2005, doi: 10.1016/j.chaos.2003.12.095.

[34] K. Biswas, S. Sen, and P. K. Dutta, "Realization of a constant phase element and its performance study in a differentiator circuit," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 9, pp. 802–806, Sep. 2006, doi: 10.1109/TCSII.2006.879102.

[35] I. Dimeas, G. Tsirimokou, C. Psychalinos, and A. S. Elwakil, "Experimental verification of filters using fractional-order capacitor and inductor emulators," in *Proc. 39th Int. Conf. Telecommun. Signal Process. (TSP)*, Vienna, Austria, Jun. 2016, pp. 559–562, doi: 10.1109/TSP.2016.7760943.

[36] D. Kubanek, J. Koton, J. Dvorak, N. Herencsar, and R. Sotner, "Optimized design of OTA-based gyrator realizing fractional-order inductance simulator: A comprehensive analysis," *Appl. Sci.*, vol. 11, no. 1, pp. 1–19, Dec. 2020, doi: 10.3390/app11010291.

[37] K. H. Khattab, A. H. Madian, and A. G. Radwan, "CFOA-based fractional order simulated inductor," in *Proc. IEEE 59th Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Abu Dhabi, United Arab Emirates, Oct. 2016, pp. 1–4, doi: 10.1109/MWSCAS.2016.7870127.

[38] A. Adhikary, S. Choudhary, and S. Sen, "Optimal design for realizing a grounded fractional order inductor using GIC," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 8, pp. 2411–2421, Aug. 2018, doi: 10.1109/TCSI.2017.2787464.

[39] J. Dvorak, D. Kubanek, N. Herencsar, A. Kartci, and P. Bertsias, "Electronically adjustable emulator of the fractional-order capacitor," *Elektronika Elektrotechnika*, vol. 25, no. 6, pp. 28–34, Dec. 2019, doi: 10.5755/j01.eie.25.6.24823.

[40] D. Goyal and P. Varshney, "Analog realization of electronically tunable fractional-order differ-integrators," *Arabian J. Sci. Eng.*, vol. 44, no. 3, pp. 1933–1948, Mar. 2019, doi: 10.1007/s13369-018-3209-z.

[41] R. Sotner, J. Jerabek, L. Langhammer, J. Koton, J. Polák, D. Andriukaitis, and A. Valinevicius, "Design of building blocks for fractional-order applications with single and compact active device," in *Proc. 43rd Int. Conf. Telecommun. Signal Process. (TSP)*, Milan, Italy, Jul. 2020, pp. 573–577, doi: 10.1109/TSP49548.2020.9163400.

[42] R. Sotner, O. Domansky, J. Jerabek, N. Herencsar, J. Petrzela, and D. Andriukaitis, "Integer- and fractional-order integral and derivative two-port summations: Practical design considerations," *Appl. Sci.*, vol. 10, no. 1, pp. 1–25, 2020, doi: 10.3390/app10010054.

[43] L. Jin, X. Li, and M. Wu, "Realization of fractional order integrator by rational function in the form of continued product," in *Proc. IEEE Int. Conf. Mechatronics Autom. (ICMA)*, Beijing, China, Aug. 2015, pp. 1630–1635, doi: 10.1109/ICMA.2015.7237729.

[44] P. Bertsias, C. Psychalinos, A. Elwakil, L. Safari, and S. Minaei, "Design and application examples of CMOS fractional-order differentiators and integrators," *Microelectron. J.*, vol. 83, pp. 155–167, Jan. 2019, doi: 10.1016/j.mejo.2018.11.013.

[45] P. Bertsias, L. Safari, S. Minaei, A. Elwakil, and C. Psychalinos, "Fractional-order differentiators and integrators with reduced circuit complexity," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2018, pp. 1–4, doi: 10.1109/ISCAS.2018.8351452.

[46] L. Langhammer, R. Sotner, J. Dvorak, O. Sladok, J. Jerabek, and P. Bertsias, "Current-mode fractional-order electronically controllable integrator design," in *Proc. 27th IEEE Int. Conf. Electron., Circuits Syst. (ICECS)*, Glasgow, U.K., Nov. 2020, pp. 1–4, doi: 10.1109/ICECS49266.2020.9294923.

[47] G. Tsirimokou and C. Psychalinos, "Ultra-low voltage fractional-order circuits using current mirrors," *Int. J. Circuit Theory Appl.*, vol. 44, no. 1, pp. 109–126, Jan. 2016, doi: 10.1002/cta.2066.

[48] M. R. Dar, N. A. Kant, and F. A. Khanday, "Realization of fractional-order double-scroll chaotic system using operational transconductance amplifier (OTA)," *J. Circuits, Syst. Comput.*, vol. 27, no. 1, pp. 1–15, 2018, doi: 10.1142/S0218126618500068.

[49] G. Tsirimokou, C. Psychalinos, and A. S. Elwakil, "Emulation of a constant phase element using operational transconductance amplifiers," *Anal. Integr. Circuits Signal Process.*, vol. 85, no. 3, pp. 413–423, Dec. 2015, doi: 10.1007/s10470-015-0626-8.

[50] R. Sotner, J. Jerabek, L. Polak, R. Prokop, and V. Kledrowetz, "Integrated building cells for a simple modular design of electronic circuits with reduced external complexity: Performance, active element assembly, and an application example," *Electronics*, vol. 8, no. 5, pp. 1–26, 2019, doi: 10.3390/electronics8050568.

[51] *Texas Instruments—OPA860—Wide Bandwidth Operational Transconductance Amplifier (Datasheet)*. Accessed: Sep. 20, 2021. [Online]. Available: https://www.ti.com/lit/ds/symlink/opa860.pdf

[52] M. Sugi, Y. Hirano, Y. F. Miura, and K. Saito, "Simulation of fractal immittance by analog circuits: An approach to the optimized circuits," *IEICE Trans. Fundamentals Electron., Commun. Comput. Sci.*, vol. E82, no. 8, pp. 1627–1634, Aug. 1999.
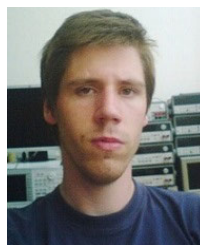
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